ST.ANNE'S COLLEGE OF ENGINEERING AND TECHNOLOGY

ANGUCHETTYPALAYAM, PANRUTI – 607 110

Department of Electronics & Communication Engineering

OBSERVATION

EC8361 – ANALOG AND DIGITAL CIRCUITS LABORATORY

STUDENT NAME :

REGISTER NO :

SEMESTER&SEC :

YEAR :

Faculty In-charge

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SYLLABUS

EC8361 ANALOG AND DIGITAL CIRCUITS LABORATORY

LIST OF ANALOG EXPERIMENTS:

1. Design of Regulated Power supplies
2. Frequency Response of CE, CB, CC and CS amplifiers
3. Darlington Amplifier
4. Differential Amplifiers- Transfer characteristic, CMRR Measurement
5. Cascode / Cascade amplifier
6. Determination of bandwidth of single stage and multistage amplifiers
7. Analysis of BJT with Fixed bias and Voltage divider bias using Spice
8. Analysis of FET, MOSFET with fixed bias, self-bias and voltage divider bias using simulation software like Spice
9. Analysis of Cascode and Cascade amplifiers using Spice
10. Analysis of Frequency Response of BJT and FET using Spice

LIST OF DIGITAL EXPERIMENTS:

11. Design and implementation of code converters using logic gates
(i) BCD to excess-3 code and vice versa (ii) Binary to gray and vice-versa
12. Design and implementation of 4 bit binary Adder/ Subtractor and BCD adder using IC 7483
13. Design and implementation of Multiplexer and De-multiplexer using logic gates
14. Design and implementation of encoder and decoder using logic gates
15. Construction and verification of 4 bit ripple counter and Mod-10 / Mod-12 Ripple counters
16. Design and implementation of 3-bit synchronous up/down counter

DESIGN OF REGULATED POWER SUPPLIES

EXPERIMENT:1 **DATE:**

AIM:

To design and construct a regulated power supplies circuit and to determine the load regulation and efficiency of the regulated power supply.

EQUIPMENTS REQUIRED

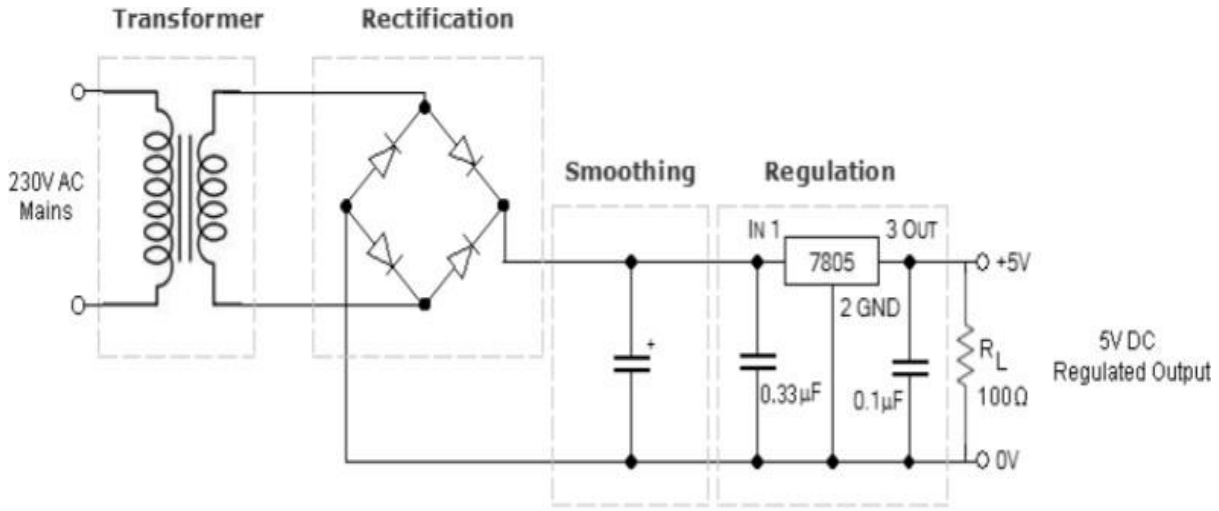
S.NO	EQUIPMENT	RANGE	QUANTITY
1	230 V/ 9 V, 1A Step down transformer	-	1
2	Diode	1N4007	1
3	IC	7805	1
4	RPS	(0-30)V	1
5	Resistor	100 Ω	1
6	Resistor	520 K	1
7	Capacitor	1000µF , 0.33µF , 0.1µF	1
8	Bread Board	-	1
9	Single strand Wires	-	-
10	CRO	(0 - 30) MHz	1
11	CRO Probes	-	3
12	Function Generator	(0 - 3) MHz	1

THEORY

- Every electronic circuit is designed to operate off of supply voltage, which is usually constant.
- A regulated power supply provides this constant DC output voltage and continuously holds the output voltage at the design value regardless of changes in load current or input voltage.
- The power supply contains a rectifier, filter, and regulator.
- The rectifier changes the AC input voltage to pulsating DC voltage.
- The filter section removes the ripple component and provides an unregulated DC voltage to the regulator section.
- The regulator is designed to deliver a constant voltage to the load under varying circuit conditions.
- The two factors that can cause the voltage across the load to vary are fluctuations in input voltage and changes in load current requirements.
- Load regulation is a measurement of power supply, showing its capacity to maintain a constant

voltage across the load with changes in load current.

- Line regulation is a measurement of power supply, showing its capacity to maintain a constant output voltage with changes in input voltage.



PROCEDURE

1. Power Supply

- Connect the circuit as shown in Figure.
- Apply 230V AC from the mains supply.
- Observe the following waveforms using oscilloscope
  (i) Waveform at the secondary of the transformer
  (ii) Waveform after rectification
  (iii) Waveform after filter capacitor
  (iv) Regulated DC output

2. Load Regulation

- Observe the No load voltage and Full load voltage
- Calculate the load regulation.
- Load Regulation = ((VNL – VFL)/VFL) x 100 %

DESIGN

Design a 5 V DC regulated power supply to deliver up to 1A of current to the load with 5% ripple. The input supply is 50Hz at 230 V AC.

Selection of Voltage regulator IC:

Fixed voltage linear IC regulators are available in a variation of voltages ranging from -24V to +24V. The current handling capacity of these ICs ranges from 0.1A to 3A. Positive fixed voltage regulator ICs have the part number as 78XX.The design requires 5V fixed DC voltage, so 7805 regulator IC rated for 1A of output current is selected.

Selection of Bypass Capacitors:

The data sheet on the 7805 series of regulators states that for best stability, the input bypass capacitor should be 0.33µF. The input bypass capacitor is needed even if the filter capacitor is used. The large electrolytic capacitor will have high internal inductance and will not function as a high frequency bypass; Therefore, a small capacitor with good high frequency response is required.
The output bypass capacitor improves the transient response of the regulator and the data sheet Recommends a value of 0.1µF.

Dropout voltage

The dropout voltage for any regulator states the minimum allowable difference between output and input voltages if the output is to be maintained at the correct level. For 7805, the dropout voltage at the input of the regulator IC is Vo +2.5 V.

Vdropout = 5+2.5 = 7.5V

- Load Regulation = ((VNL – VFL)/VFL) x 100 %

TABULATION

S.No	Output V_{AC}	Output V_{DC}	Theoretical Ripple factor	Practical Ripple factor	Output voltage without regulator	Output voltage without regulator

LOAD REGULATION

S.No	**R_L**	**Vo**

RESULT

Hence designed and constructed the regulated power supply and the load regulation are calculated.

FREQUENCY RESPONSE OF COMMON EMITTER AMPLIFIER

EXPERIMENT:2A **DATE:**

AIM:

To design and construct a common emitter amplifier circuit and to determine its bandwidth and cut off frequency.

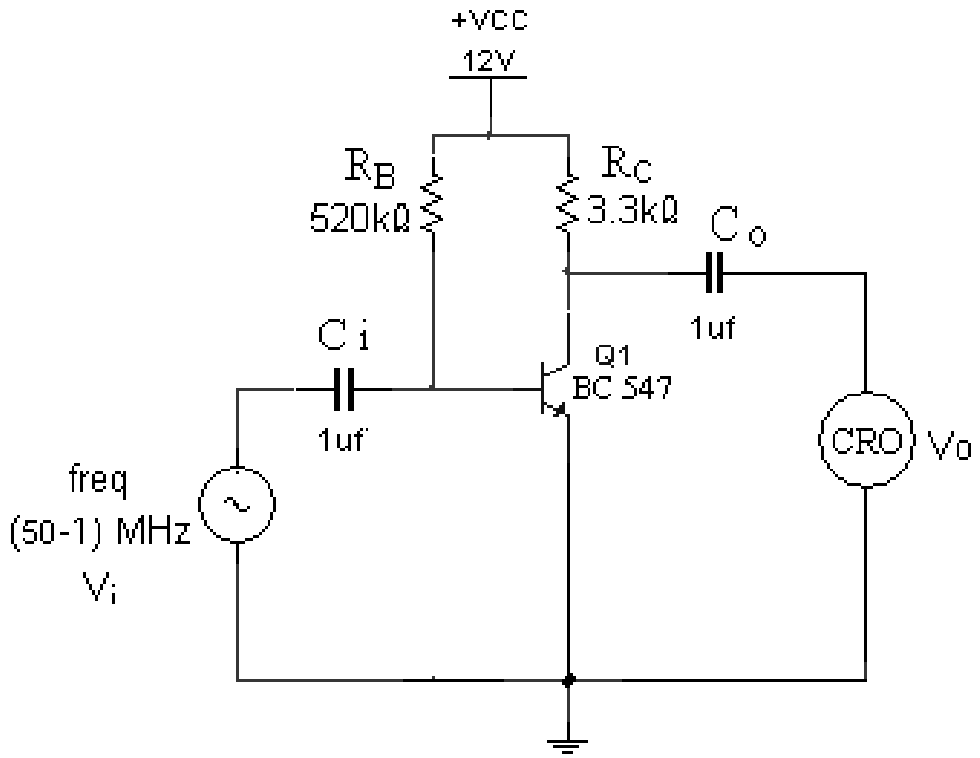
EQUIPMENTS REQUIRED

S.NO	EQUIPMENT	RANGE	QUANTITY
1	Transistor	BC 547	1
2	RPS	(0-30)V	1
3	Resistor	3.3 K	1
4	Resistor	520 K	1
5	Capacitor	1 uf	2
6	Bread Board	-	1
7	Single strand Wires	-	-
8	CRO	(0 - 30) MHz	1
9	CRO Probes	-	3
10	Function Generator	(0 - 3) MHz	1

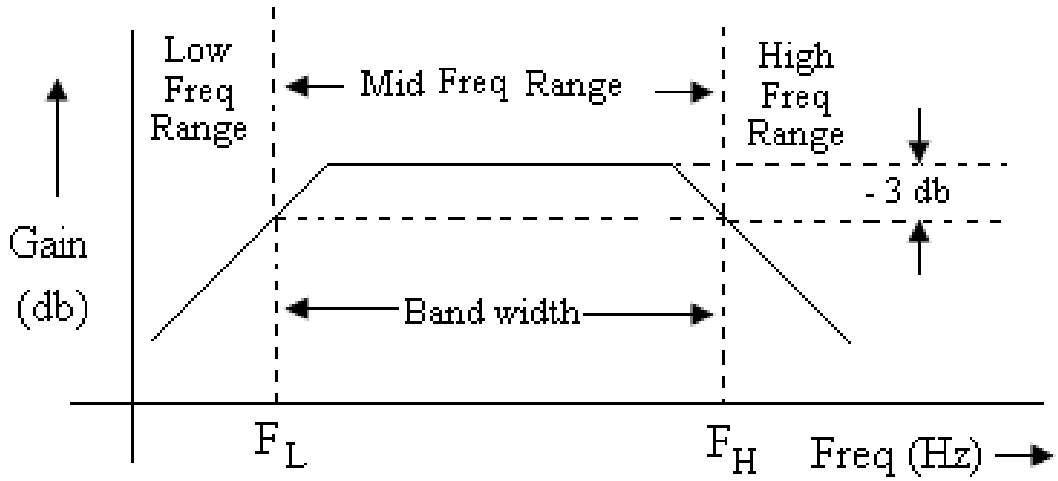
PROCEDURE

1. Connect the circuit as per the circuit diagram
2. Set Vs = 50mV using signal generator.
3. Keep the input voltage constant; vary the frequency from 50 Hz to 1 MHz in steps.
4. Note down the corresponding output voltage.
5. Plot the graph gain Vs frequency.
6. Calculate the bandwidth from the graph.

Common Emitter Amplifier using Fixed Bias



Model Graph



THEORY

An amplifier is used to increase the signal level; the amplifier is use to get a larger signal output from a small signal input The transistor can be used as a amplifier, if it is biased to operate in the active region, i.e. base-emitter junction is to be forward biased, while the base –collector junction to be reverse biased. Common-emitter amplifier is constructed using fixed bias circuit. The resistors R_C and R_B are biasing resistors. The input AC signal is given to the base of the transistor. The capacitors Ci and Co are coupling capacitors. The output is taken between the collector terminal and ground.

DESIGN OF FIXED BIAS COMMON EMITTER AMPLIFIER

Design parameters

Vcc=12V, Ic =Ie=2mA, h_{fe} (β) =100, Vbe =0.7V, V_{CE} = 6V

To find Rc

Apply KVL to collector loop
Vcc-IcRc-Vce = 0
Rc = Vcc-Vce / Ic
Rc = 12 - 6 / $4x10^{-3}$
Rc = 3 kΩ

To find R_B

Apply KVL to base loop
$Vcc-I_bR_b-V_{be} = 0$
$R_b = Vcc-V_{be} / I_b$
$R_b = 12 – 0.7 / 20x10^{-6}$
R_b = 565 kΩ

To find C_i (Input capacitor)

$X_{Ci} = R_B \| h_{ie} / 10$

X_{Ci} = 565KΩ || 1.3 KΩ
X_{Ci} = (565KΩ * 1.3 KΩ / 565KΩ +1.3 KΩ) / 10
X_{Ci} = 129
$X_{Ci} = 1 / 2\pi f C_i$
Let f=1000
$C_i = 1 / 2\pi f X_{Ci}$
$C_i = 1 / 2*\pi *1000* 129$
C_i = 1.2 µf use approx 1 µf

$h_{ie} = \beta r_e$ (where r_e internal emitter resistance)
$r_e = 26mV / I_E$
$r_e = 26mV / 2mA$
$r_e = 13$

$h_{ie} = \beta r_e$
h_{ie} =100 * 13 =1300
h_{ie} = 1300 Ω or 1.3 KΩ

TABULATION

Vin = _____

SL.NO		Frequency (Hz)	Output Voltage (Vo)	Gain = 20 log (Vo / Vi) (db)

To find C_O (Output capacitor)

Assume R_L =4.7 K

$X_{CO} = R_C \parallel R_L / 10$

R_C =3 KΩ & R_L = 4.7 KΩ

X_{CO} = (3KΩ * 4.7 KΩ / 3KΩ +4.7 KΩ) / 10

X_{CO} = 183

$X_{Ci} = 1 / 2\pi f C_O$

Let f=1000

$C_O = 1 / 2\pi f X_{CO}$

$C_O = 1 / 2*\pi *1000* 183$

$C_O = 0.83$ µf use approx 1 µf

RESULT

Hence designed and constructed the Common Emitter Amplifier using fixed bias and calculated the band width and cut-off frequency.

FREQUENCY RESPONSE OF COMMON COLLECTOR AMPLIFIER

EXPERIMENT:2B **DATE:**

AIM:

To design and construct a common collector amplifier and to calculate the bandwidth and cut off frequency.

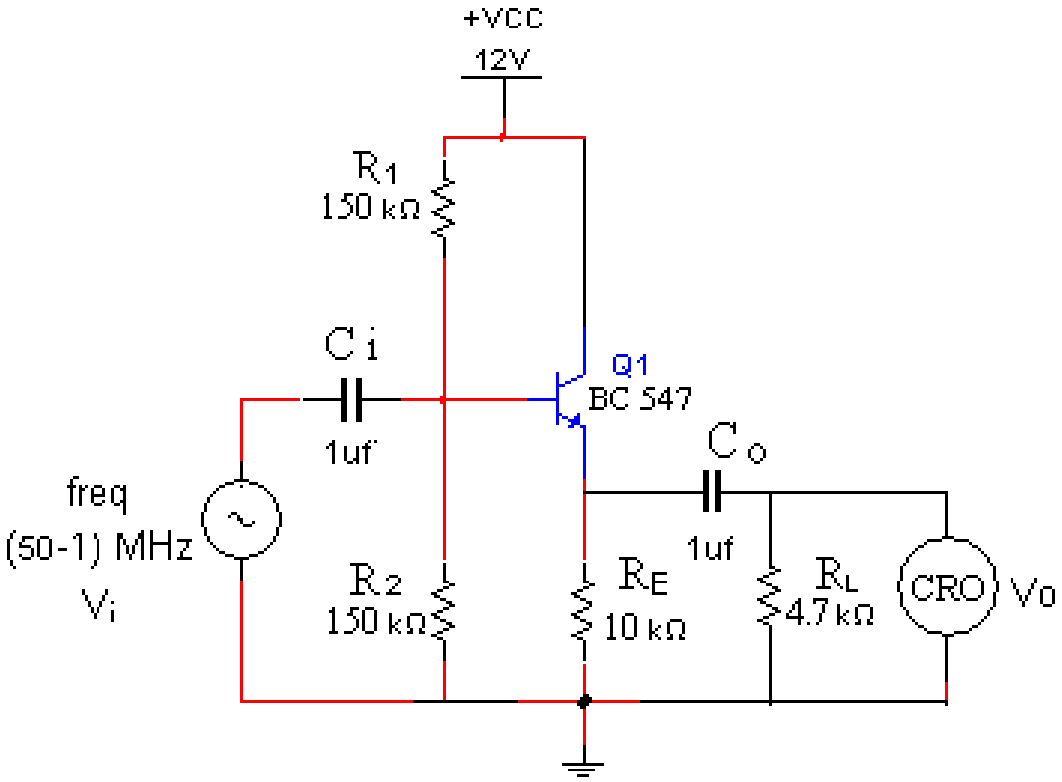
EQUIPMENTS REQUIRED

S.NO	EQUIPMENT	RANGE	QUANTITY
1	Transistor	BC 547	1
2	RPS	(0-30)V	1
3	Resistor	150 K Ω	2
4	Resistor	10 K Ω	1
5	Resistor	4.7K Ω	1
6	Resistor	1.2 K	1
7	Capacitor	1 uf	2
8	Bread Board	-	1
9	Single strand Wires	-	-
10	CRO	(0 - 30) MHz	1
11	CRO Probes	-	3
12	Function Generator	(0 - 3) MHz	1

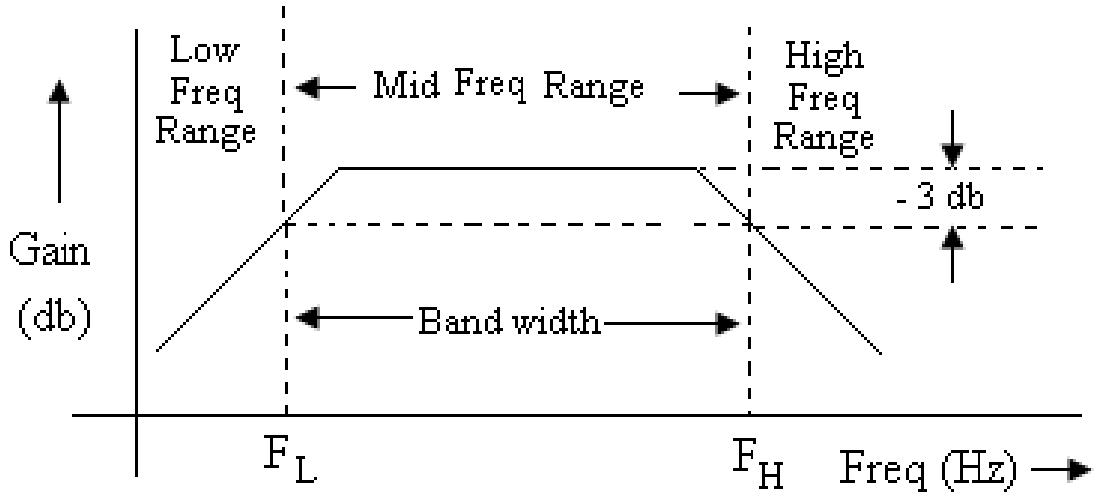
PROCEDURE

1. Connect the circuit as per the circuit diagram
2. Set Vs = 2V using signal generator.
3. Keep the input voltage constant; vary the frequency from 50 Hz to 1 MHz in steps.
4. Note down the corresponding output voltage.
5. Plot the graph gain Vs frequency.
6. Calculate the bandwidth from the graph.

Common collector Amplifier



Model Graph



THEORY

The d.c biasing in common collector is provided by R_1, R_2 and R_E .The load resistance is capacitor coupled to the emitter terminal of the transistor.

When a signal is applied to the base of the transistor , V_B is increased and decreased as the signal goes positive and negative, respectively. Considering V_{BE} is constant the variation in the V_B appears at the emitter and emitter voltage V_E will vary same as base voltage V_B . Since the emitter is output terminal, it can be noted that the output voltage from a common collector circuit is the same as its input voltage. Hence the common collector circuit is also known as an emitter follower.

DESIGN OF COMMON COLLECTOR AMPLIFIER

Design parameters

Vcc=12V, Ie=2mA, h_{fe} (β) =100, Vbe =0.7V, S=10, R_L4.7 kΩ

Design specifications

Vcc – V_{CE}-V_E =0

V_{CE} =50% of Vcc

V_{CE} =0.5 * 12 =6 V

V_E=12- 6

V_E=6V

To find R_{eff}

$V_E = I_E * R_{eff}$

$R_{eff} = V_E / I_E$

$R_{eff} = 6 / 2x10^{-3}$

R_{eff}= 3 KΩ

To find R_E

$R_{eff} = R_E \parallel R_L$

3 KΩ = R_E*4.7KΩ / R_E+4.7KΩ

R_E = 8.2 KΩ use approx 10 KΩ

TABULATION

Vin = _____

SL.NO	Frequency (Hz)	Output Voltage (Vo)	Gain = 20 log (Vo / Vi) (db)

For determining the values of R_1 & R_2 ($R_B = R_1 || R_2$) following steps should be followed
Step 1 : Calculate R_B
Step 2 : Calculate V_{TH}

Let

$R_B = R_1 \| R_2$
$R_B = R_1 * R_2 / R_1 + R_2$ ---------- (1)
$V_{TH} = Vcc * R_2 / R_1 + R_2$ ----------(2)

Calculation of R_B
From Approx analysis
$S = 1 + (R_B / R_E)$
$10 = 1 + R_B / 8.2\ K\Omega$
$9 * 8.2\ K\Omega = R_B$
$R_B = 73\ K\Omega$

Calculation of V_{TH}
$V_{TH} - V_{BE} - V_E = 0$
$V_{TH} = V_{BE} + V_E$
$V_{TH} = 0.7 + 6$
$V_{TH} = 6.7\ V$

From eqn (2)
$V_{TH} / Vcc = R_2 / R_1 + R_2$
$6.7 / 12 = R_2 / R_1 + R_2$
$0.558 = R_2 / R_1 + R_2$ ---------- (3)

To find R_1
From (1)
$R_B = R_1 * R_2 / R_1 + R_2$
$7300 = 0.558 * R_1$
$R_1 = 130\ k\Omega$ use approx $150\ k\Omega$

To find R_2

From (3)
$0.558 = R_2 / R_1 + R_2$
$0.558 (R_1 + R_2) = R_2$
$0.558 (130 x 10^3 + R_2) = R_2$
$R_2 = 162\ k\Omega$ use approx $150\ k\Omega$

CALCULATION

RESULT

Hence designed and constructed the Common collector Amplifier and calculated the band width and cut-off frequency.

DESIGN OF COMMON BASE AMPLIFIER CIRCUIT

EXPERIMENT:2C **DATE:**

AIM:

To design and construct a Common Base amplifier circuit using and to calculate its bandwidth and cut off frequency.

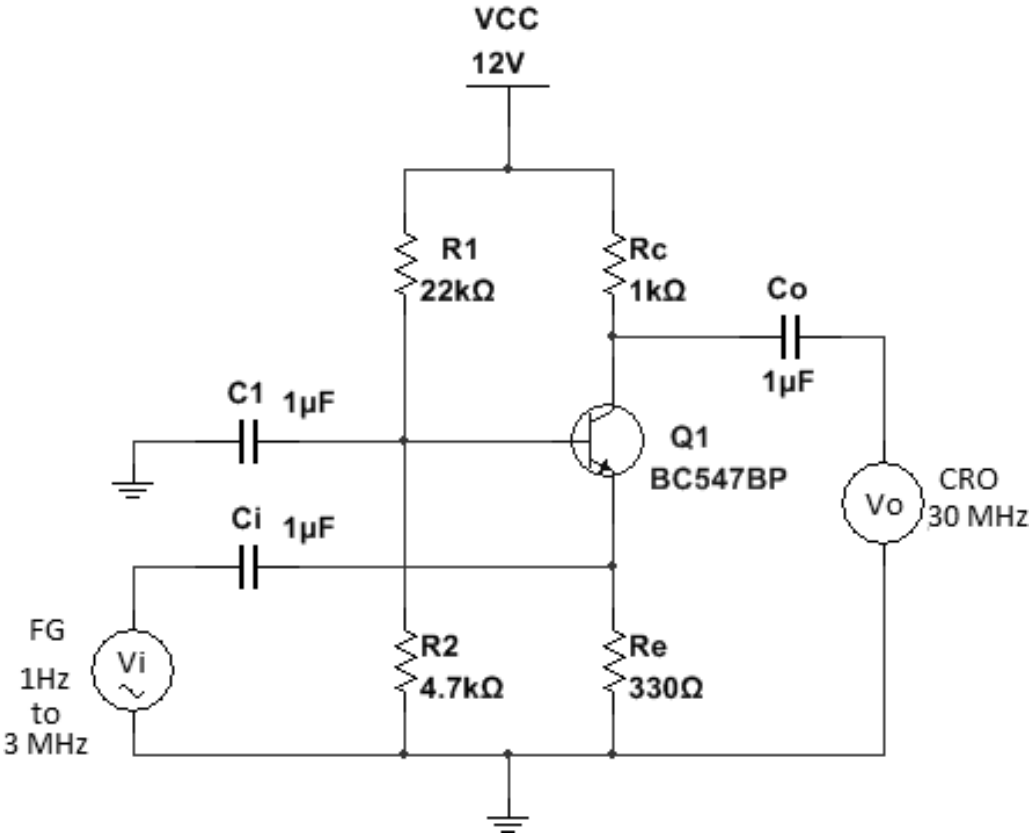
EQUIPMENTS REQUIRED

S.NO	EQUIPMENT	RANGE	QUANTITY
1	Transistor	BC 547	1
2	RPS	(0-30)V	1
3	Resistor	22 K	1
4	Resistor	4.7 K	1
5	Resistor	330 Ω	1
6	Resistor	1.2 K	1
7	Capacitor	1 uf	3
8	Bread Board	-	1
9	Single strand Wires	-	-
10	CRO	30 MHz	1
11	CRO Probes	-	3
12	Function Generator	(0 - 3) MHz	1

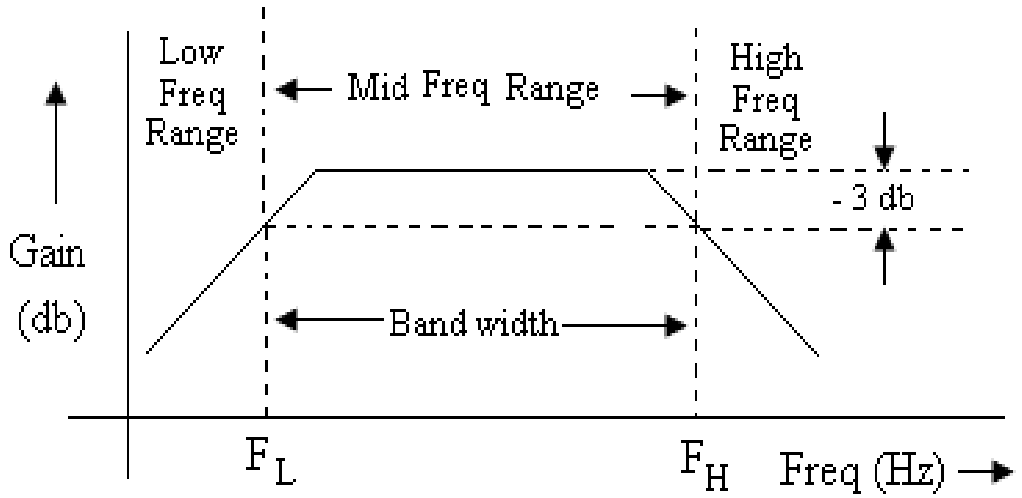
PROCEDURE

1. Connect the circuit as per the circuit diagram
2. Set Vs = 50mV using signal generator.
3. Keep the input voltage constant; vary the frequency from 50 Hz to 3 MHz in steps.
4. Note down the corresponding output voltage.
5. Plot the graph gain Vs frequency.
6. Calculate the bandwidth from the graph.

Common Base Amplifier Circuit



Model Graph



THEORY

An amplifier is used to increase the signal level; the amplifier is use to get a larger signal output from a small signal input The transistor can be used as a amplifier, if it is biased to operate in the active region, i.e. base-emitter junction is to be forward biased, while the base –collector junction to be reverse

biased. Common-Base amplifier is constructed using self-bias circuit. The resistors R_1, R_2 and R_E are biasing resistors. Acts as a potential divider. Due to the change in the temperature or β, the base current increases so this makes to increase the collector current I_C, therefore a Reverse Leakage Current I_{CO} increases hence this affects the stability of transistor. By providing an emitter resistor R_E, it creates a voltage drop across R_E therefore the increased emitter current due to I_C starts to flow through R_E to ground and this makes in the reduction of Base Emitter Voltage V_{BE}. Due to reduction in V_{BE}, base current I_B reduces and hence collector Current I_C also reduces and the output remains constant.

For the common base amplifier the AC Input resistance is typically low from 10 to 100Ω. The output resistance of CB amplifier is typically high from 50KΩ to 1MΩ. Typical values of voltage amplification (Av) for CB amplifier vary from 50 to 300. The current amplification is always less than 1.The basic CB amplifying action was proposed for transferring the current from low resistance to high resistance circuit.

DESIGN OF COMMON BASE AMPLIFIER

Design parameters

Vcc=12V, Ic =Ie=4mA, h_{fe} (β) =100, Vbe =0.7V, S=10

Design specifications

Vcc =12V

V_{RE} =10% of Vcc

V_{RC} =40% of Vcc

V_{CE} =50% of Vcc

Ic =Ie

Ib =Ic / β

V_{RE} =10% of Vcc

V_{RE} =0.1 * 12 =1.2 V

V_{RC} =40% of Vcc

V_{RC} =0.4 * 12 =4.8 V

V_{CE} =50% of Vcc

V_{CE} =0.5 * 12 =6 V

To find R_E

$R_E = V_{RE} / Ie$

$R_E = 1.2 / 4x10^{-3}$

$R_E = 300\ \Omega$

TABULATION

Vin = _____

SL.NO	Frequency (Hz)	Output Voltage (Vo)	Gain = 20 log (Vo / Vi) (db)

To find Rc

Apply KVL to collector loop
Vcc-IcRc-Vce – IeRe = 0 IeRe =V_{RE}
Vcc-IcRc-Vce – V_{RE} = 0
Rc = Vcc-Vce – V_{RE} / Ic
Rc = 12 - 6 – 1.2 / $4x10^{-3}$
Rc = 1.2 kΩ

For determining the values of R_1 & R_2 ($R_B = R_1 || R_2$) following steps should be followed
Step 1 : Calculate R_B
Step 2 : Calculate V_{TH}

Let
$R_B = R_1 || R_2$
$R_B = R_1 * R_2 / R_1 + R_2$---------- (1)
$V_{TH} = Vcc * R_2 / R_1 + R_2$----------(2)

Calculation of R_B
From Approx analysis
$S = 1 + (R_B / R_E)$
$10 = 1 + R_B / 300$
$9 * 300 = R_B$
$R_B = 2700$

Calculation of V_{TH}
$V_{TH} - V_{BE} - V_{RE} = 0$
$V_{TH} = V_{BE} + V_{RE}$
$V_{TH} = 0.7 + 1.2$
$V_{TH} = 1.9V$

From eqn (2)
$V_{TH} / Vcc = R_2 / R_1 + R_2$
$1.9 / 12 = R_2 / R_1 + R_2$
$0.158 = R_2 / R_1 + R_2$---------- (3)

Sub (3) in (1)
$R_B = R_1 * R_2 / R_1 + R_2$
$2700 = 0.158 * R_1$
$R_1 = 17\ k\Omega$ use approx $22\ k\Omega$
From (3)
$0.158 = R_2 / R_1 + R_2$
$0.158 (R_1 + R_2) = R_2$
$0.158 (17 \times 10^3 + R_2) = R_2$
$R_2 = 3.2\ k\Omega$ use approx $4.7\ k\Omega$

To find C_i (Input capacitor)

$X_{Ci} = R_B || h_{ie} / 10$

$X_{Ci} = 4.1K\Omega || 1.3\ K\Omega$
$X_{Ci} = (4.1K\Omega * 1.3\ K\Omega / 4.1K\Omega + 1.3\ K\Omega) / 10$
$X_{Ci} = 98$
$X_{Ci} = 1 / 2\pi f C_i$
Let f=1000
$C_i = 1 / 2\pi f X_{Ci}$
$C_i = 1 / 2 * \pi * 1000 * 98$

$C_i = 1.6\ \mu f$ use approx 1 µf

To find C_O (Output capacitor)

$X_{CO} = R_C \parallel R_L / 10$
Let $R_C = 1\ K\Omega$ & $R_L = 4.7\ K\Omega$
$X_{CO} = (1K\Omega * 4.7\ K\Omega / 1K\Omega + 4.7\ K\Omega) / 10$
$X_{CO} = 82$
$X_{Ci} = 1 / 2\pi f C_O$
Let f=1000
$C_O = 1 / 2\pi f X_{CO}$
$C_O = 1 / 2*\pi *1000* 82$
$C_O = 1.9\ \mu f$ use approx 1 µf

RESULT

Hence designed and constructed the Common Base Amplifier and calculated the band width and cut-off frequency.

S

COMMON-SOURCE AMPLIFIER

EXPERIMENT:2D **DATE:**

AIM:

To design and construct a common-source amplifier circuit and to determine its frequency response.

COMPONENTS & EQUIPMENTS REQUIRED:

S.NO	COMPONENT	RANGE	QUANTITY
1	Transistor	BFW 10	1
2	RPS	(0-30)V	1
3	Signal Generator	(0-3)MHz	1
4	CRO	(0-30)MHz	1
5	Bread Board	-	1
6	Resistors	10K, 2.2K, 3.3M	1
7	Capacitors	0.1uf	2
8	Single strand Wires	-	-
9	CRO Probes	-	3

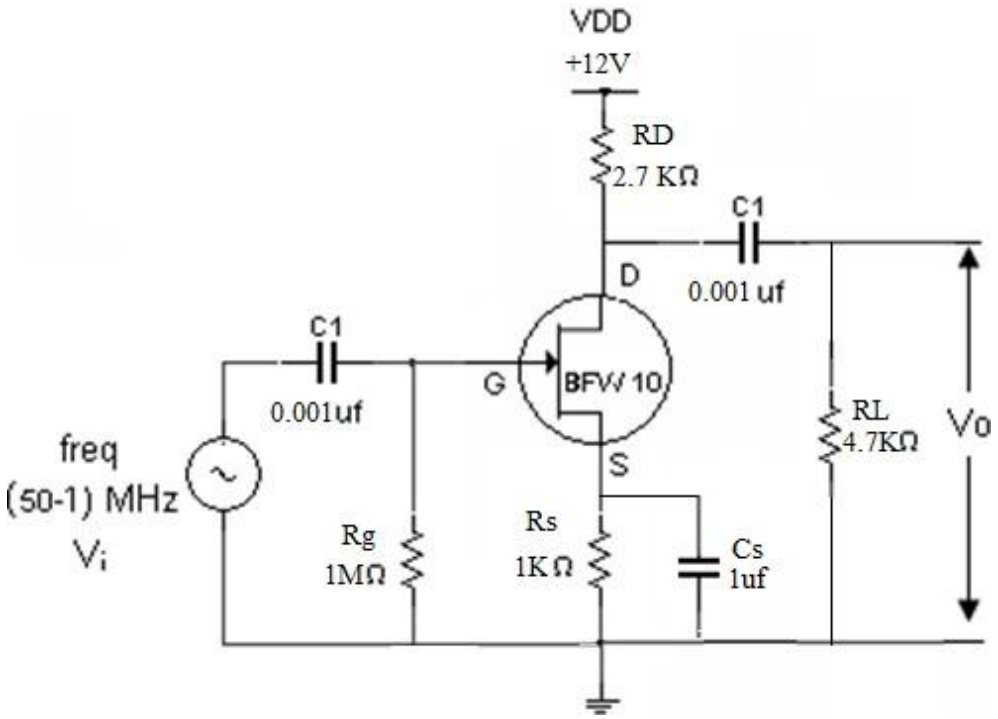
PROCEDURE:

1. Connect the circuit diagram as per the circuit diagram.
2. Set Vi = 50mV, using the signal generator.
3. Keeping the input voltage constant, Vary the frequency from 0 Hz to 1 MHz in regular steps and note down the corresponding output voltage.
4. Plot the graph: Gain (dB) vs Frequency (Hz)
5. Calculate the bandwidth from the graph.

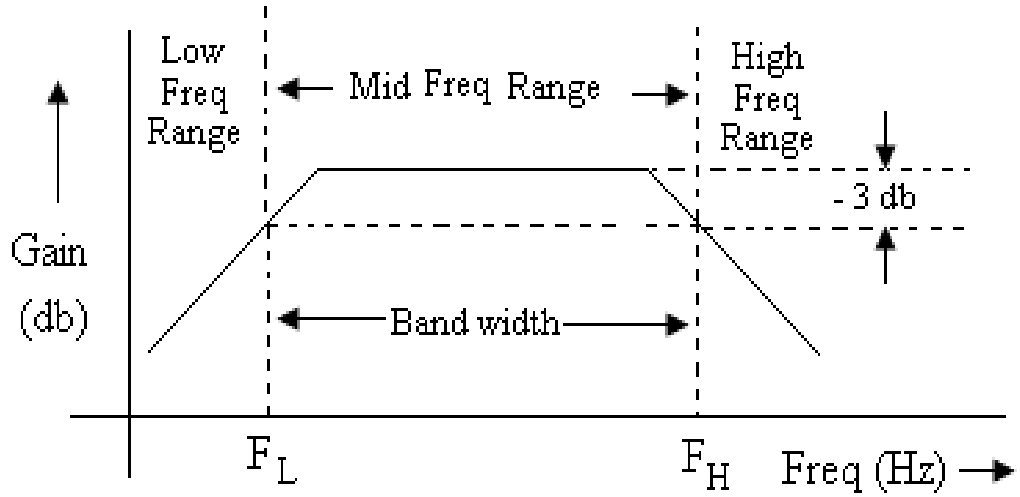
THEORY :

The common source configuration for a FET is similar to the common emitter bipolar transistor configuration, The common source amplifier can provide both a voltage and current gain. Since the input resistance looking into the gate is extremely large the current gain available from the FET amplifier can be quite large, but the voltage gain is generally inferior to that available from a bipolar device. Thus FET amplifiers are most useful with high output-impedance signal sources where a large current gain is the primary requirement. The source by-pass capacitor provides a low impedance path to ground for high frequency components and hence AC signals will not cause a swing in the bias voltage.A basic common-source amplifier circuit containing an N-channel JFET. The characteristics of this circuit include high input impedance and a high voltage gain. The function of the circuit components are C1 and C2 are the input and output coupling capacitors. Rg is the gate return resistor.

CIRCUIT DIAGRAM OF COMMON SOURCE AMPLIFIER



Model Graph



Design Specifications

V_{DD}=12V, V_{GS}=-2V, for N-Channel JFET (BFW10) Ro=40K, and g_m=2.5mA/V at I_D=2mA, and V_P=8V

Design of Rg

Select Rg=1MΩ (since voltage across Rg assumed to be 0V)

Design of R_D

V_{RD}=45% of V_{DD} = 5.4V

$V_{RD}=I_d*R_D$

RD= V_{RD}/I_d= 2.7KΩ

Design of R_S

Rs=V_{RS}/I_S =V_{RS}/I_D ($I_D=I_S$=2mA)

V_{RS}=Vg-VGS

V_{RS} =0-(-2V) =2V

RS=$2/2*10^{-3}$=1KΩ

Design of R_L

Gain of CS amp A=gm($R_D \| R_L$)

The required gain=15

R_L=4.7KΩ

To find C_S (Bypass capacitor)

X_{CS} =R_S / 10 =1000 /10 =100

X_{CS} =100

X_{CS} =1 / 2π f C_S

Let f=1000

C_S = 1 / 2π f X_{CS}

C_S = 1 / 2*π *1000* 100

C_S = 1 µf

To find C_i (Input capacitor)

X_{Ci} =Rg /10=0.1MΩ

X_{Ci} =1 / 2π f C_i

Let f=1000

C_i = 1 / 2π f X_{Ci}

C_i = 1 / 2*π *1000* 0.1MΩ

C_i = 0.001 µf

To find C_O (Output capacitor)

X_{CO} =R_S / 10 = 100

X_{CO} =1 / 2π f C_O

Let f=1000

C_O = 1 / 2π f X_{CO}

C_O = 1 / 2*π *1000* 1000

C_O =1.5 µf use approx 1 µf

TABULATION:

S.NO	Frequency in Hz	Vo in Volts	Gain : 20 Log(Vo/Vin)

RESULT:

Thus the common source amplifier has been constructed, and frequency response of the amplifier has drawn.

DARLINGTON AMPLIFIERS

EXPERIMENT:3 **DATE:**

AIM:

To design and construct a darlington amplifier and to calculate the bandwidth and cut off frequency.

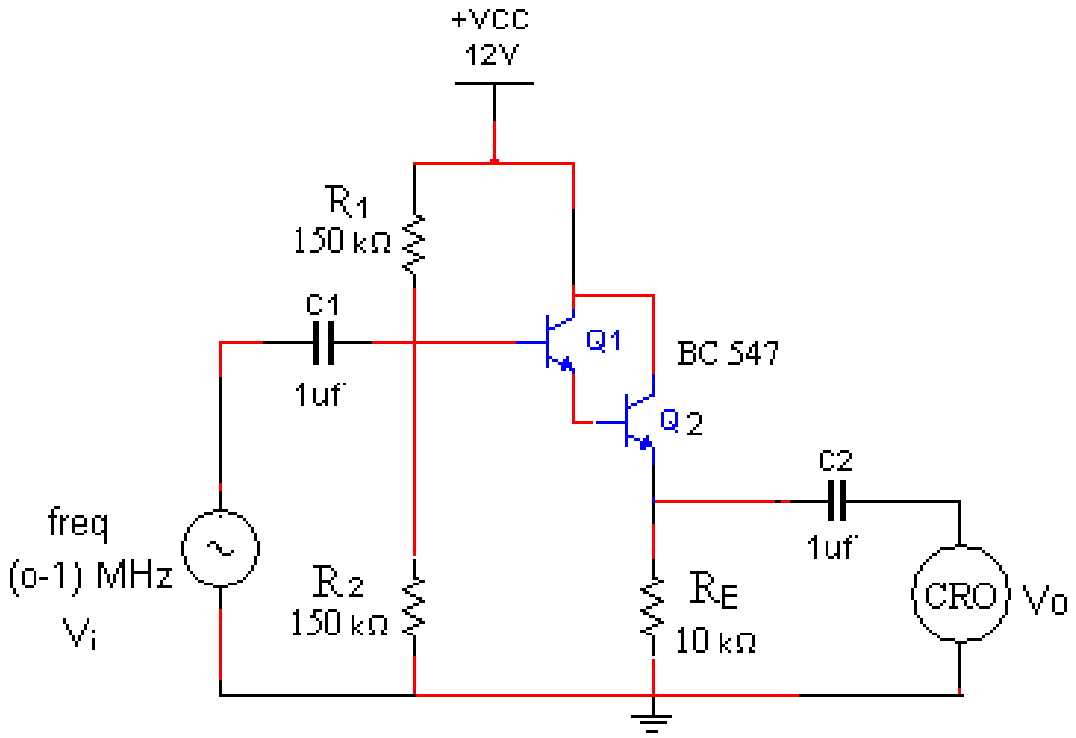
EQUIPMENTS REQUIRED

S.NO	EQUIPMENT	RANGE	QUANTITY
1	Transistor	BC 547	2
2	RPS	(0-30)V	1
3	Resistor	150 K Ω	2
4	Resistor	10 K Ω	1
5	Resistor	4.7K Ω	1
6	Capacitor	1 uf	2
7	Bread Board	-	1
8	Single strand Wires	-	-
9	CRO	(0 - 30) MHz	1
10	CRO Probes	-	3
11	Function Generator	(0 - 3) MHz	1

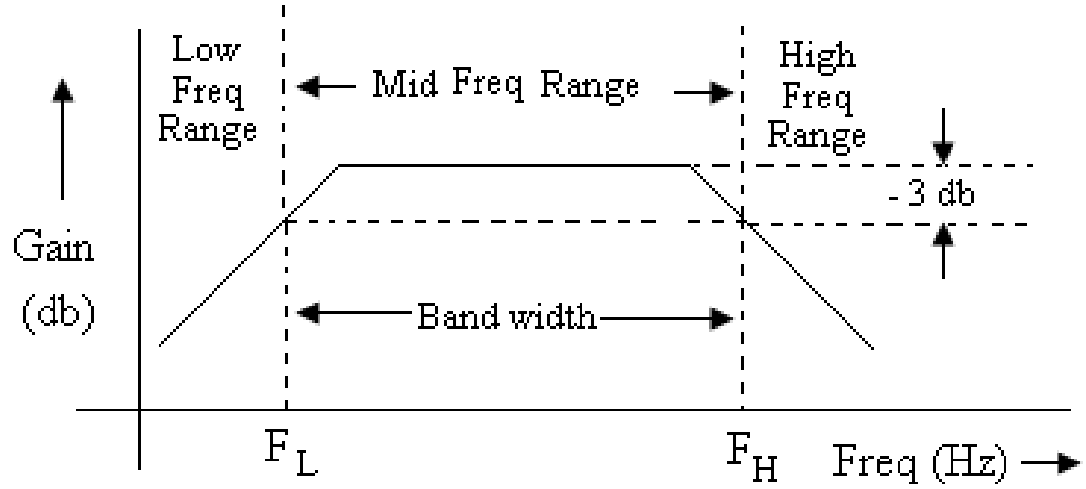
PROCEDURE

1. Connect the circuit as per the circuit diagram
2. Set Vs = 2V using signal generator.
3. Keep the input voltage constant; vary the frequency from 50 Hz to 1 MHz in steps.
4. Note down the corresponding output voltage.
5. Plot the graph gain Vs frequency.
6. Calculate the bandwidth from the graph.

Darlington Amplifier



Model Graph



THEORY

In Darlington connection of transistors, emitter of the first transistor is directly connected to the base of the second transistor .Because of direct coupling dc output current of the first stage is $(1+h_{fe})I_{b1}$.If Darlington connection for n transitor is considered, then due to direct coupling the dc output

current foe last stage is $(1+h_{fe})^{n}$ times I_{b1} .Due to very large amplification factor even two stage Darlington connection has large output current and output stage may have to be a power stage. As the power amplifiers are not used in the amplifier circuits it is not possible to use more than two transistors in the Darlington connection.

In Darlington transistor connection, the leakage current of the first transistor is amplified by the second transistor and overall leakage current may be high, Which is not desired.

DESIGN OF DARLINGTON AMPLIFIER

Design parameters

Vcc=12V, Ie=2mA, h_{fe} (β) =100, Vbe =0.7V, S=10, R_L4.7 kΩ

Design specifications

Vcc – V_{CE}-V_E =0

V_{CE} =50% of Vcc

V_{CE} =0.5 * 12 =6 V

V_E=12- 6

V_E=6V

To find R_{eff}

$V_E = I_E * R_{eff}$

$R_{eff} = V_E / I_E$

$R_{eff} = 6 / 2x10^{-3}$

R_{eff}= 3 KΩ

To find R_E

$R_{eff} = R_E \parallel R_L$

3 KΩ = R_E*4.7KΩ / R_E+4.7KΩ

R_E = 8.2 KΩ use approx 10 KΩ

TABULATION

Vin = _____

SL.NO	Frequency (Hz)	Output Voltage (Vo)	Gain = 20 log (Vo / Vi) (db)

For determining the values of R_1 & R_2 ($R_B = R_1 || R_2$) following steps should be followed
Step 1 : Calculate R_B
Step 2 : Calculate V_{TH}

Let
$R_B = R_1 || R_2$
$R_B = R_1 * R_2 / R_1 + R_2$---------- (1)
$V_{TH} = Vcc * R_2 / R_1 + R_2$----------(2)

Calculation of R_B

From Approx analysis

$S = 1+ (R_B / R_E)$

$10 = 1 + R_B / 8.2\ K\Omega$

$9*8.2\ K\Omega = R_B$

$R_B = 73\ K\Omega$

Calculation of V_{TH}

$V_{TH} - V_{BE} - V_E = 0$

$V_{TH} = V_{BE} + V_E$

$V_{TH} = 0.7 + 6$

$V_{TH} = 6.7\ V$

From eqn (2)

$V_{TH} / Vcc = R_2 / R_1+R_2$

$6.7 / 12 = R_2 / R_1+R_2$

$0.558 = R_2 / R_1+R_2$---------- (3)

To find R_1

From (1)

$R_B = R_1*R_2 / R_1+R_2$

$7300 = 0.558 * R_1$

$R_1 = 130\ k\Omega$ use approx 150 kΩ

To find R_2

From (3)

$0.558 = R_2 / R_1+R_2$

$0.558 (R_1+R_2) = R_2$

$0.558 (130x10^3 + R_2) = R_2$

$R_2 = 162\ k\Omega$ use approx 150 kΩ

CALCULATION

RESULT

Hence designed and constructed the darlington Amplifier and calculated the band width and cut- off frequency

DIFFERENTIAL AMPLIFIERS

EXPERIMENT:4 **DATE:**

AIM

To construct a differential amplifier circuit for single input balanced output in the common mode and differential mode configuration and study the output waveform and to find Common Mode Rejection Ratio (CMRR).

EQUIPMENTS REQUIRED

S.NO	EQUIPMENT	RANGE	QUANTITY
1	Transistor	BC 107	2
2	Dual trace Regulated power supply	(0-30)V	1
3	Resistor	10 K	2
4	Resistor	4.7 k	1
5	Function Generator	(0-3)MHz	1
6	Bread Board	-	1
7	Single strand Wires	-	-
8	CRO	(0-30)MHz	1
9	CRO Probes	-	4

PROCEDURE

Differential mode configuration :

1. Connections are given as per circuit diagram
2. Set Vs =50 mV, using signal generator
3. Keeping the input voltage constant vary the frequency from 50Hz to1MHz in regular steps
4. Observe both input and output on the CRO (sine wave)
5. The differential gain is calculated at mid frequency range where the magnitude of the sine wave is maximum.
6. The differential gain is calculated by Ad = Vo / Vi

Common mode configuration

1. Connections are given as per circuit diagram
2. Set Vs =50 mV, using signal generator
3. Keeping the input voltage constant vary the frequency from 50Hz to1MHz in regular steps
4. Observe both input and output on the CRO (sine wave)
5. The common mode gain is calculated at mid frequency range where the magnitude of the sine wave is maximum.

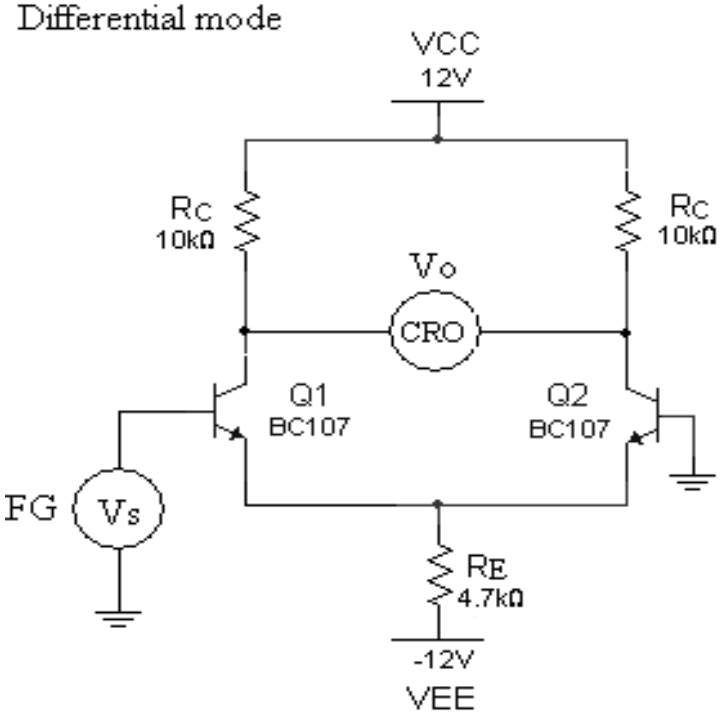
6. The Common mode gain is calculated by Ac = Vo / Vi

CMRR

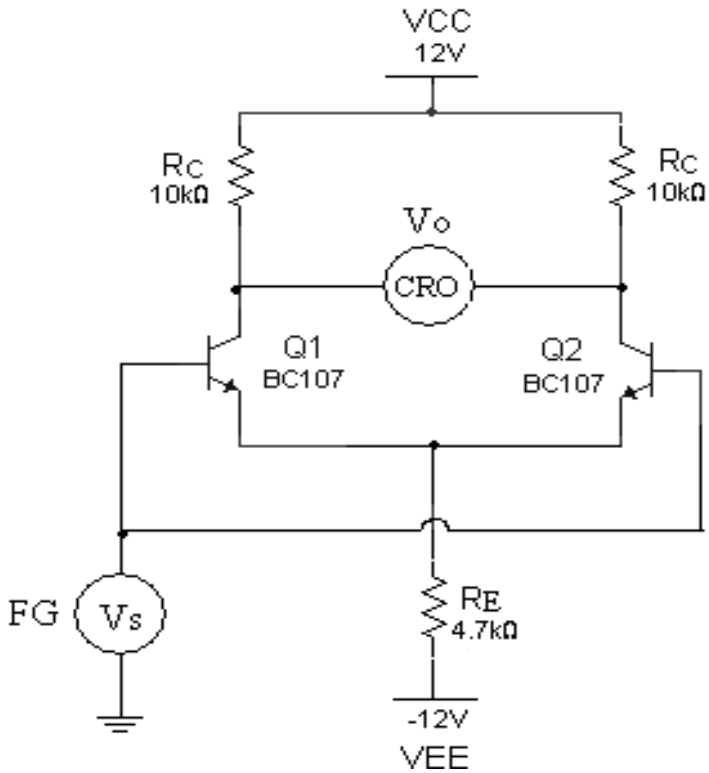
1. CMRR is calculated by substituting the practical values of Ad and Ac in the formula
   CMRR = 20 log (A_D / Ac)

Single input Balanced output Differential Amplifier

Differential mode



Common mode



THEORY

The Differential amplifier amplifies the difference between two input signals. The transistorized differential amplifier consists of two ideal emitter biased circuits. The differential amplifier circuit is obtained by connecting the two emitter terminals E_1 and E_2. Hence RE is the parallel combination of R_{E1} and R_{E2}. The output is taken between the two collector terminals C_1 and C_2.Hence we say this connection as balanced output or double ended output. It works in two modes of operation.

Differential mode operation

In the differential mode operation two input signals (V_1 and V_2) are different in magnitudes and opposite in phase and it produces the difference between the two input signals (V_1~V_2).The differential mode gain (A_D) can be calculated by $A_D = Rc * \beta / 2* h_{ie.}$

Common mode operation

In the common mode operation two input signals are same in magnitude and phase. At emitter resistance R_E both the input signal appears across R_E and adds together since it just acts like an emitter follower .Therefore R_E carries a signal current and provides a negative feedback. This feedback reduces the common mode gain of the differential amplifier. The Common mode gain Ac can be calculated by

$|Ac| = Rc * \beta / h_{ie} + (2Re [1+ \beta])$

CMRR

CMRR (Common Mode Rejection Ratio) is defined as the ratio of differential gain to common mode gain. Ideally the CMRR should be infinity. $CMRR = 20 \log (A_D / Ac)$

TABULATION

DIFFERENTIAL MODE

S.NO	Input Amplitude (Vi) (Volts)	Output Amplitude (Vo) (Volts)	Theoretical Differential gain (Ad)	Practical Differential gain (Vo / Vi) (Ad)

COMMON MODE

S.NO	Input Amplitude (Vi) (Volts)	Output Amplitude (Vo) (Volts)	Theoretical Differential gain (Ac)	Practical Differential gain (Vo / Vi) (Ac)

CMRR

S.NO	Theoretical CMRR	**Practical CMRR** = 20 log (A_D / Ac)

DIFFERENTIAL AMPLIFIER

Design parameters
Vcc=12V, Vee = -12V, $Ic_1 = Ic_1$ = 2mA, Ie=4mA, h_{fe} (β) =300, Vbe =0.7V, h_{ie} =4.7kΩ

To find Rc

Apply KVL to collector loop
Vcc-IcRc-Vce-IeRe – Vee =0
Rc = {Vcc- Vce - V_{RE} - Vee }/ Ic
= {12-6 -1.2 –(-12)} /2x10^{-3}
Rc = 8.7kΩ use approx 10 kΩ

NOTE

Vcc =12V
V_{RE} =10% of Vcc =0.1 * 12 = 1.2 V
V_{RC} =40% of Vcc =0.4 * 12 = 4.8 V
V_{CE} =50% of Vcc =0.5 * 12 = 6 V
$Ic_1 = Ic_1$ = 2mA

To find Rc

Apply KVL to collector loop
Vcc-IcRc-Vce-IeRe – Vee =0
Re = {Vcc- V_{RC} – Vce - Vee}/ Ie
= {12 - 4.8 – 6 – (-12)} /4x10^{-3}
Re = 3.3 kΩ use approx 4.7kΩ

Differential gain

A_D =Rc * β / 2* h_{ie}
A_D =8.7x10^3 * 300 / 2* 4.7 x10^3
A_D = 265

Common mode gain

|Ac| = Rc * β / h_{ie} + (2Re [1+ β])
Ac = 8.7kΩ * 300 / 4.7 kΩ + (2 * 3.3 kΩ [1+ 300])
Ac = 1.2

CMRR
Theoretical CMRR = 20 log (A_D / Ac)
= 20 log (265 / 1.2)
= 46

CALCULATION:

RESULT

Thus constructed a differential amplifier circuit for single input balanced output in the common mode and differential mode configuration and studied the output waveform, also its CMRR has been determined and verified practically.

Differential mode : _____

Common mode : _____

CMRR : _____

CASCODE AMPLIFIERS

EXPERIMENT:5A **DATE:**

AIM:

To design and construct a cascode amplifier circuit and to draw its frequency response graph.

EQUIPMENTS REQUIRED

S.NO	EQUIPMENT	RANGE	QUANTITY
1	Transistor	BC 547	2
2	RPS	(0-30)V	1
3	Resistor	1.2K, 33 K,22K, 12K	1
4	Resistor	680Ω	1
5	Capacitor	1 uf, 2.2uf	2
6	Bread Board	-	1
7	Single strand Wires	-	-
8	CRO	(0 - 30) MHz	1
9	CRO Probes	-	3
10	Function Generator	(0 - 3) MHz	1

PROCEDURE

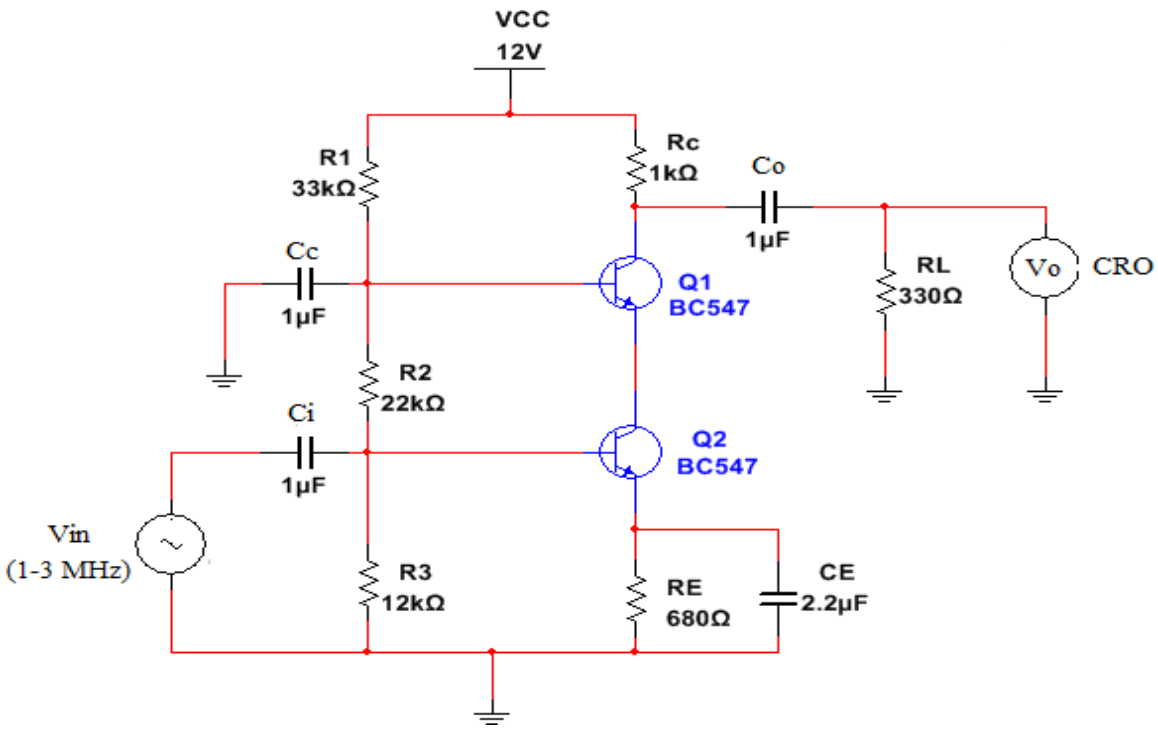
1. Connect the circuit as per the circuit diagram
2. Set Vs = 50mV using signal generator.
3. Keep the input voltage constant; vary the frequency from 50 Hz to 1 MHz in steps.
4. Note down the corresponding output voltage.
5. Plot the graph gain Vs frequency.

Calculate the bandwidth from the graph

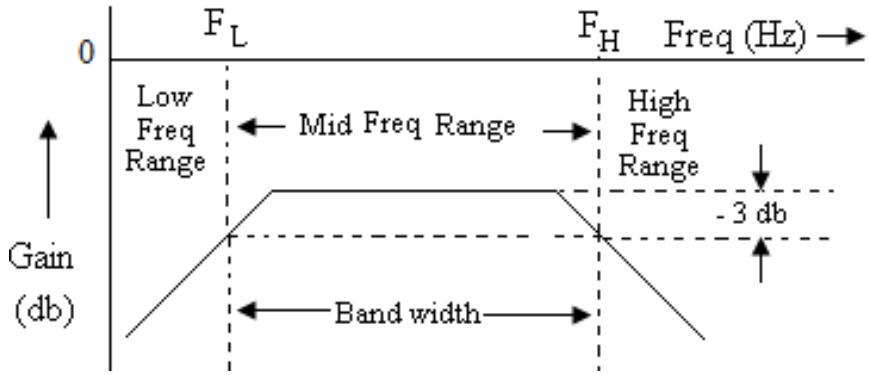
THEORY

A cascode amplifier comprises of a common emitter amplifier and a common base amplifier stages in cascade. In the circuit diagram Q1 common base configuration and Q2 is common emitter configuration. Principal advantage of this circuit is its low internal capacitance which is a limiting factor gain at high frequencies. Cascode amplifier can able to amplify wide range of frequencies than that is possible with CE amplifier. This is because no high frequency feedback occurs from the output back to input through the miller capacitance as it occurs in transistor CE configuration. Cascode amplifier provides same voltage gain of CE amplifier but in wide range of frequencies. The advantage of CE and CB stages are put together in cascode connection.

CASCODE AMPLIFIER CIRCUIT DIAGRAM



Model Graph



DESIGN OF FIXED BIAS COMMON EMITTER AMPLIFIER

Design parameters
Vcc=12V, Ic =2mA, h_{fe} (β) =100, Vbe =0.7V,
V_{CE1}= V_{CE2}=35% of Vcc = 4.2V
V_{RE}=10% of V_{CC} =1.2V
V_{RC}=20% of V_{CC}=2.4V

To find Rc

V_{RC} =Ic*Rc =2.4V
Rc=1.2KΩ

To find R_E

$V_{RE} = I_E * R_E = 1.2V$
$R_E = 600\Omega$

To find R_1, R_2 and R_3
$Vcc - V_{R1} - V_{BE1} - V_{CE2} - V_{RE} = 0$
$V_{R1} = Vcc - V_{BE1} - V_{CE2} - V_{RE}$
$V_{R1} = 12 - 0.6 - 4.2 - 12 = 6V$
$I_B = Ic/Hfe = 20\mu A$
If $10I_B$ assumed flowing through R_1 we get
$R1 = V_{R1}/10\ I_B = 30K\Omega$

$Vcc - V_{R1} - V_{R2} - V_{BE2} - V_{RE} = 0$
$V_{R2} = Vcc - V_{R1} - V_{BE2} - V_{RE}$
$V_{R2} = 12 - 6 - 0.6 - 1.2 = 4.2V$
$I_B = Ic/Hfe = 20\mu A$
If $9I_B$ assumed flowing through R_2 we get
$R2 = V_{R2}/9\ I_B = 23K\Omega$

$V_{R3} - V_{BE2} - V_{RE} = 0$
$V_{R3} = V_{BE2} + V_{RE}$
$V_{R3} = 0.6 + 1.2 = 1.8V$
$I_B = Ic/Hfe = 20\mu A$
If $8I_B$ assumed flowing through R_3 we get
$R3 = V_{R3}/8\ I_B = 11.2K\Omega$

To find C_E (Bypass capacitor)
$X_{CE} = R_E / 10$
$X_{CE} = 600\Omega / 10 = 60$
$X_{CE} = 1 / 2\pi f C_E$ Let f=1000
$C_E = 1 / 2*\pi *1000* 60 = 2.2\ \mu f$

TABULATION

Vin = _____

SL.NO	Frequency (Hz)	Output Voltage (Vo)	Gain = 20 log (Vo / Vi) (db)

RESULT

Hence designed and constructed Cascode amplifier and plotted its frequency response.

CASCADE AMPLIFIER

EXPERIMENT:5B **DATE:**

AIM:

To Design and Construct a Cascade Amplifier and to determine its:

a. DC Characteristics

b. Maximum Signal Handling Capacity

c. Gain of the amplifier

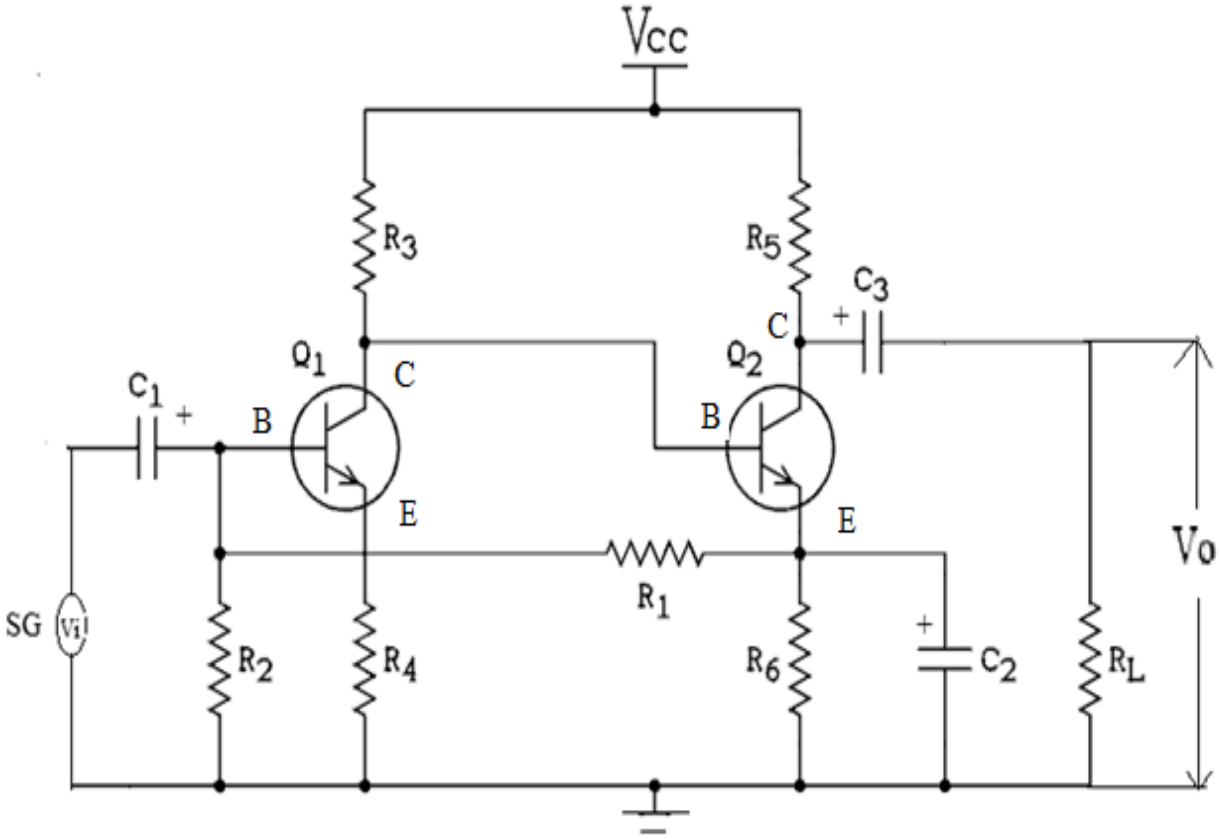
d. Bandwidth of the amplifier

e. Gain -Bandwidth Product

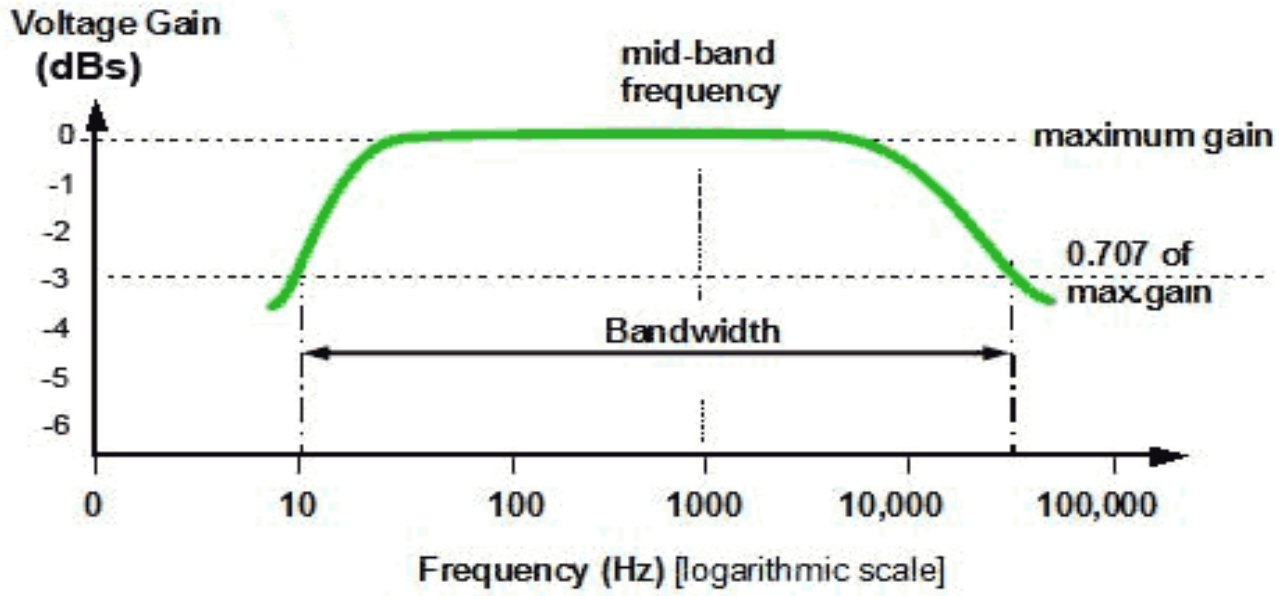
REQUIREMENTS:

S.NO	REQUIREMENT	NAME	RANGE	QUANTITY
1	**COMPONENTS**	Transistor [Active]	BFW10	1
2		Resistor [Passive]		
3		Capacitor [Passive]		
4	**EQUIPMENTS**	Signal Generator	(0-3)MHz	1
5		CRO	30MHz	1
6		Regulated power supply	(0-30)V	1
7	**ACESSORIES**	Bread Board	-	1
8		Connecting Wires	Single strand	as required

Cascade amplifier Circuit Diagram:



MODEL GRAPH:



DESIGN PROCEDURE:

Given specifications:

VCC= 14 V, IC1=1.2mA, RL = 40KΩ hFE= 100

(i) To calculate R5 :

Assume VE1 = 5V , VCE1 = VCE2 = 3V;

VB2 = VC1 = VE1 + VCE1 = 5V + 3V = 8V

VE2 = VB2 – VBE = 8V – 0.7V = 7.3V

VR5 = Vcc – VE2 – VCE2 = 14V – 7.3V – 3V = 3.7V

Choose R5 = RL / 10 = 40KΩ / 10 = 4KΩ ;

IC2 = (VR5 / R5) = 3.7V / 3.9KΩ = 1000μA

(ii) To calculate R6 :

VR6 = VE2 / IC2 = 7.7KΩ;

IC2 = VE2 / R6 = 7.3V / 8.2 KΩ = 890μA

(iii) To calculate R1, R2 , R3 & R4:

Voltage across resistor R3 is given by

VR3 = Vcc – VC1 = 14V – 8V = 6V

R3 = VR3 / IC1 = 6V / 1mA = 6KΩ

R4 = VE1 / IC1 = 5V/ 1mA = 4.7KΩ

Voltage across resistor R2 is given by

VR2 = VE1 – VBE = 5V + 0.7V =5.7V

R2 = 10 R4 = 4.7 KΩ

VR1 = VCC – VB1 = 14V + 5.7V =8.3V

R1 = [VR1 x R2 / VR2] = 68.4 KΩ

THEORY:

A cascade is type of multistage amplifier where two or more single stage amplifiers are connected serially. Many times the primary requirement of the amplifier cannot be achieved with single stage amplifier, because Of the limitation of the transistor parameters. In such situations more than one amplifier stages are cascaded such that input and output stages provide impedance

matching requirements with some amplification and remaining middle stages provide most of the amplification. These types of amplifier circuits are employed in designing microphone and loudspeaker.

PROCEDURE:

1. Connect the circuit as per the circuit diagram
2. Determine the Q-point of the amplifier using DC analysis.
3. Determine Maximum input voltage that can be applied to amplifier using AC analysis.
4. Set the input voltage Vin=V MSH /2 and vary the input signal frequency from 0Hz to 1MHz in incremental steps and note down the corresponding output voltage Vo for atleast 20 different values for the considered range.
5. The voltage gain is calculated as Av = 20log (V0/Vi)
6. Find the Bandwidth and Gain-Bandwidth Product from Semi-log graph taking

frequency on x-axis and gain in dB on y-axis.,

Bandwidth, BW = f2-f1 where f1 - lower cut-off frequency

f2 - upper cut-off frequency

a. DC ANALYSIS:

It is the procedure to find the operating region of transistor

Steps:

I) Set Vin = 0 by reducing the amplitude of the input signal from signal generator
II) Open circuit the capacitors since it blocks DC voltage
III) Set V_{CC}= +10v and measure the voltage drop across the Resistor V_{RC}, voltage across Collector- Emitter Junction V_{CE} and Voltage drop across base emitter junction. V_{BE}
IV) Find the Q-point of the transistor and draw the DC load line.

To verify dc condition
1. V_{BE} : (forward bias)
2. V_{RC} = _____
3. V_{CE} = _____ (REVERSE BIAS)
4. Ic(Ic = (Vcc – V_{CE}) / Rc) =_____

Q point analysis:

It is the procedure to choose the opearating point of transistor

Q-point: (I_{CQ} =_____ ; V_{CEQ} =_____)

b. Maximum signal handling capacity:

It is the process to find the maximum input voltage that can be handled by the amplifier, so that it amplifies the input signal without any distortion.

Procedure:

i. Apply input signal Vin = 20 mV of 1Khz frequency to the amplifier using the signal generator between base emitter junction of the transistor. Find the sinusoidal output using CRO across RL.

ii. By increasing the amplitude of the input signal find maximum input voltage V_{MSH} across V_{BE} at which the sinusoidal signal gets distorted during the process which can be seen in the CRO. The amplitude obtained at this point is maximum voltage that can be applied to the transistor for efficient operating of transistor.

V_{MSH} = _____ volts

TABULATION

Input voltage (Vin=V_{MSH}/2) =_____ volts

S. NO	FREQUENCY [Hz]	OUTPUT VOLTAGE [VO] in Volts	GAIN= 20 log vo/vin dB
1	0		
2	100		
3	500		
4	600		
5	800		
6	900		
7	1KHz		
8	100 KHz		
9	500 KHz		
10	600 KHz		
11	700 KHz		
12	800 KHz		
13	900 KHz		
14	1MHz		
15	1.1 MHz		
16	1.5 MHz		

RESULT:

The Cascade amplifier was constructed and input resistance and gain were determined. The results are found to be as given below

a) Gain of the amplifier:

b) Bandwidth of the amplifier:

c) Gain-Bandwidth product:

DETERMINATION OF BANDWIDTH OF SINGLE STAGE AND MULTISTAGE AMPLIFIERS USING BJT

EXPERIMENT:6 **DATE:**

AIM:

To determine the bandwidth of single stage and multistage amplifier circuit using BJT and to plot its frequency response.

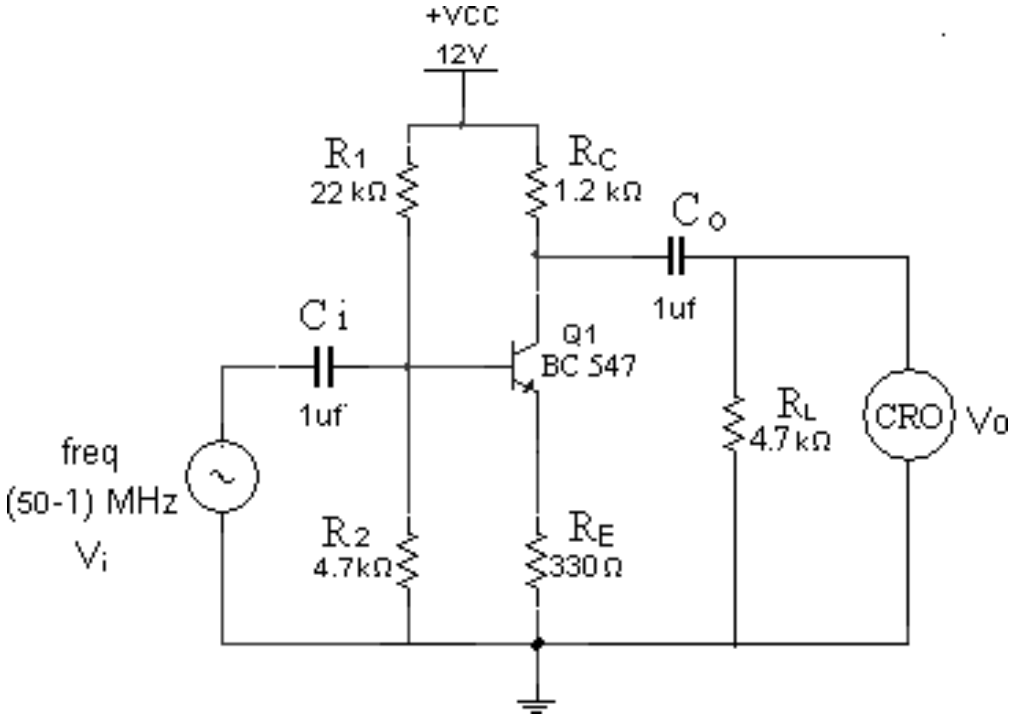
EQUIPMENTS REQUIRED

S.NO	EQUIPMENT	RANGE	QUANTITY
1	Transistor	BC 547	2
2	RPS	(0-30)V	1
3	Resistor	22 K	2
4	Resistor	4.7 K	2
5	Resistor	330 Ω	2
6	Resistor	1.2 K	2
7	Capacitor	1 uf, 4.7uf	3 2
8	Bread Board	-	1
9	Single strand Wires	-	-
10	CRO	30 MHz	1
11	CRO Probes	-	3
12	Function Generator	(0 - 3) MHz	1

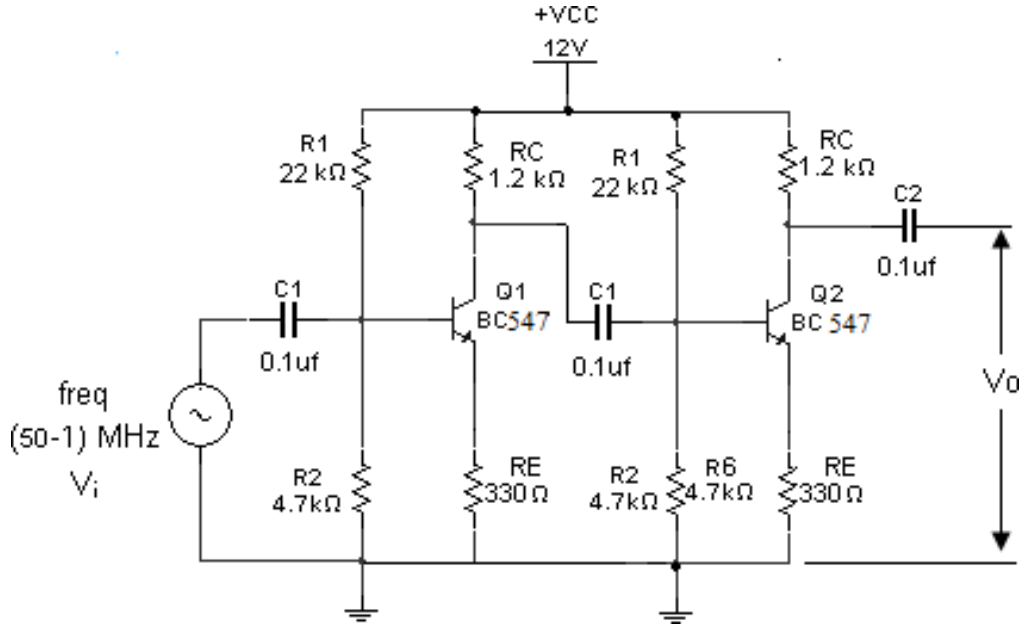
PROCEDURE

1. Connect the circuit as per the circuit diagram
2. Set Vs = 50mV using signal generator.
3. Keep the input voltage constant; vary the frequency from 50 Hz to 1 MHz in steps.
4. Note down the corresponding output voltage.
5. Plot the graph gain Vs frequency
6. Calculate the bandwidth from the graph

SINGLE STAGE AMPLIFIER CIRCUIT USING BJT



MULTISTAGE AMPLIFIER CIRCUIT (CASCADE AMPLIFIER CIRCUIT)



THEORY

Single Stage amplifier

An amplifier is used to increase the signal level; the amplifier is use to get a larger signal output from a small signal input The transistor can be used as a amplifier, if it is biased to operate in the active

region, i.e. base-emitter junction is to be forward biased, while the base –collector junction to be reverse biased. Common-emitter amplifier is constructed using self bias circuit. The resistors R_1, R_2 and R_E are biasing resistors.

The resistors R_1 and R_2 act as a potential divider giving a fixed voltage to the base of the transistor. Due to the change in the temperature or β, the base current increases so this makes to increase the collector current $I_{C,}$ therefore a Reverse Leakage Current I_{CO} increases hence this affects the stability of transistor. By providing an emitter resistor R_E, it creates a voltage drop across R_E therefore the increased emitter current due to I_C starts to flow through R_E to ground and this makes in the reduction of Base Emitter Voltage V_{BE}. Due to reduction in V_{BE}, base current I_B reduces and hence collector Current I_C also reduces and the output remains constant.

Multistage amplifier

Rc coupled amplifier usually employed for voltage amplification. It consists of a coupling capacitor which is used to connect the output of the first stage to the base (ie input) of the next stage. The resistors R1, R2, RE forms the biasing and stabilizing network. The emitter bypass capacitor offers low resistance path to the signal. Without it, the voltage gain of the each stage would be lost. The coupling capacitor blocks DC and allows AC therefore this prevents the DC interference between the various stages and the shifting of operating point.

When AC signal is applied to the base of the first transistor, it appears in the amplified form across its collector load Rc. the amplified signal developed across Rc is given to the next stage through coupling capacitor. The second stage does further amplification of the signal, in this way the cascaded stages amplify the signal and the overall gain is considerably increased and the bandwidth decreases.

DESIGN OF COMMON EMITTER AMPLIFIER

Design parameters

Vcc=12V, Ic =Ie=4mA, h_{fe} (β) =100, Vbe =0.7V, S=10

Design specifications

Vcc =12V

V_{RE} =10% of Vcc

V_{RC} =40% of Vcc

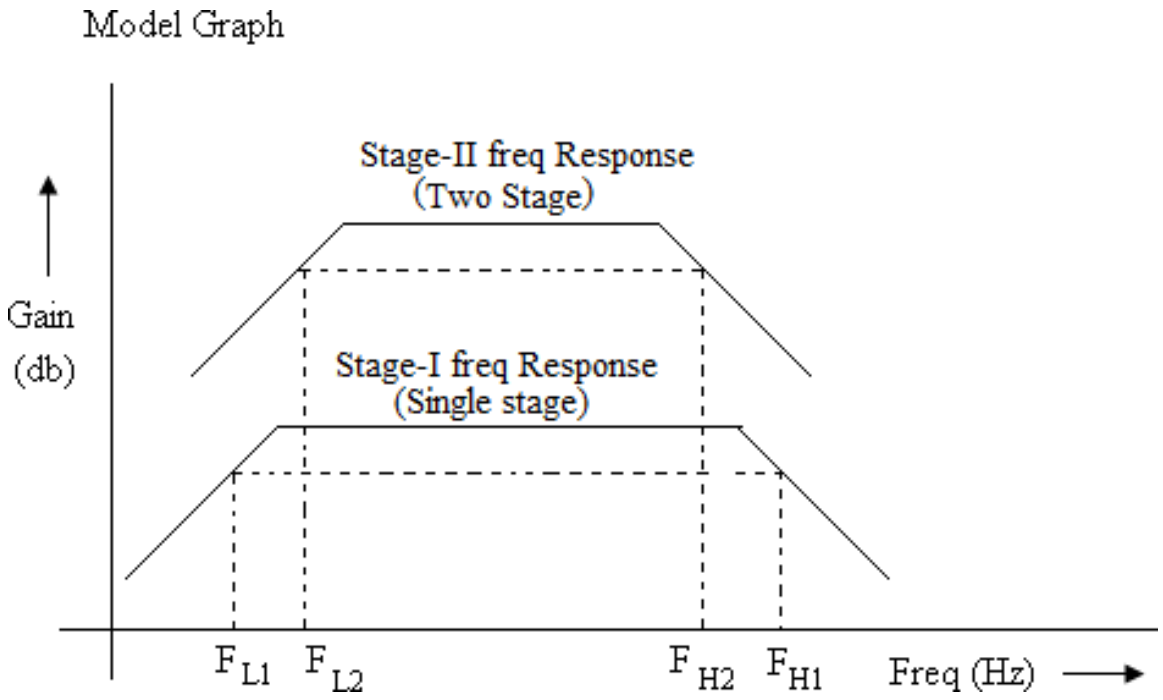
V_{CE} =50% of Vcc

Ic =Ie

Ib =Ic / β

V_{RE} =10% of Vcc

FREQUENCY RESPONSE BETWEEN SINGLE STAGE AND MULTISTAGE AMPLIFIER



V_{RE} =0.1 * 12 =1.2 V
V_{RC} =40% of Vcc
V_{RC} =0.4 * 12 =4.8 V
V_{CE} =50% of Vcc
V_{CE} =0.5 * 12 =6 V
To find R_E
$R_E = V_{RE} / Ie$
$R_E = 1.2 / 4x10^{-3}$
R_E = 300 Ω
To find Rc
Apply KVL to collector loop
Vcc-IcRc-Vce – IeRe = 0 IeRe =V_{RE}
Vcc-IcRc-Vce – V_{RE} = 0
$Rc = Vcc-Vce – V_{RE} / Ic$
$Rc = 12 - 6 – 1.2 / 4x10^{-3}$
Rc = 1.2 kΩ
For determining the values of R_1 & R_2 ($R_B = R_1 || R_2$) following steps should be followed
Step 1 : Calculate R_B
Step 2 : Calculate V_{TH}
Let
$R_B = R_1 || R_2$
$R_B = R_1 * R_2 / R_1 + R_2$---------- (1)
$V_{TH} = Vcc * R_2 / R_1 + R_2$---------- (2)
Calculation of R_B
From Approx analysis
$S = 1 + (R_B / R_E)$
$10 = 1 + R_B / 300$
$9 * 300 = R_B$
R_B =2700
Calculation of V_{TH}

$V_{TH} - V_{BE} - V_{RE} = 0$
$V_{TH} = V_{BE} + V_{RE}$
$V_{TH} = 0.7 + 1.2$; $V_{TH} = 1.9V$

TABULATION
SINGLE STAGE AMPLIFIER

Vin = _____

SL.NO	Frequency (Hz)	Output Voltage (Vo)	Gain = 20 log (Vo / Vi) (db)

TABULATION
SINGLE STAGE AMPLIFIER

Vin = _____

SL.NO	Frequency (Hz)	Output Voltage (Vo)	Gain = 20 log (Vo / Vi) (db)

From eqn (2)
$V_{TH} / Vcc = R_2 / R_1 + R_2$

$1.9 / 12 = R_2 / R_1+R_2$
$0.158 = R_2 / R_1+R_2$---------- (3)
Sub (3) in (1)
$R_B = R_1*R_2 / R_1+R_2$
$2700 = 0.158 * R_1$
$R_1 = 17\ k\Omega$ use approx 22 kΩ
From (3)
$0.158 = R_2 / R_1+R_2$
$0.158 (R_1+R_2) = R_2$
$0.158 (17 x10^3 + R_2) = R_2$
$R_2 = 3.2\ k\Omega$ use approx 4.7 kΩ

To find C_E (Emitter capacitor or Bypass capacitor)

$X_{CE} = R_E / 10 = 330 / 10 = 33$
$X_{CE} = 33$
$X_{CE} = 1 / 2\pi f C_E$
Let f=1000
$C_E = 1 / 2\pi f X_{CE}$
$C_E = 1 / 2*\pi *1000* 33$
$C_E = 4.7\ \mu f$

To find C_i (Input capacitor)

$X_{Ci} = R_B \parallel h_{ie} / 10$

$X_{Ci} = 4.1K\Omega \parallel 1.3\ K\Omega$
$X_{Ci} = (4.1K\Omega * 1.3\ K\Omega / 4.1K\Omega + 1.3\ K\Omega) / 10$
$X_{Ci} = 98$
$X_{Ci} = 1 / 2\pi f C_i$
Let f=1000
$C_i = 1 / 2\pi f X_{Ci}$
$C_i = 1 / 2*\pi *1000* 98$
$C_i = 1.6\ \mu f$ use approx 1 µf

To find C_O (Output capacitor)
$X_{CO} = R_C \parallel R_L / 10$
Let $R_C = 1\ K\Omega$ & $R_L = 4.7\ K\Omega$
$X_{CO} = (1K\Omega * 4.7\ K\Omega / 1K\Omega + 4.7\ K\Omega) / 10$
$X_{CO} = 82$

$R_B = R_1 \parallel R_2$
$R_B = 33k* 4.7k / 33k* 4.7k$
$R_B = 4.1K\Omega$

$h_{ie} = \beta\ r_e$ (where r_e internal emitter resistance)
$r_e = 26mV / I_E$
$r_e = 26mV / 2mA$
$r_e = 13$

$h_{ie} = \beta\ r_e$
$h_{ie} = 100 * 13$
$h_{ie} = 1300\ \Omega$ or $1.3\ K\Omega$

$X_{Ci} = 1 / 2\pi f C_O$
Let f=1000
$C_O = 1 / 2\pi f X_{CO}$
$C_O = 1 / 2*\pi *1000* 82$
$C_O = 1.9\ \mu f$ use approx 1 µf

RESULT

Hence designed and constructed the single stage and multistage Amplifier and calculated its band width and cut-off frequency.

SIMULATION USING PSPICE

COMMON EMITTER AMPLIFIER

EXPT NO:08 **DATE:**

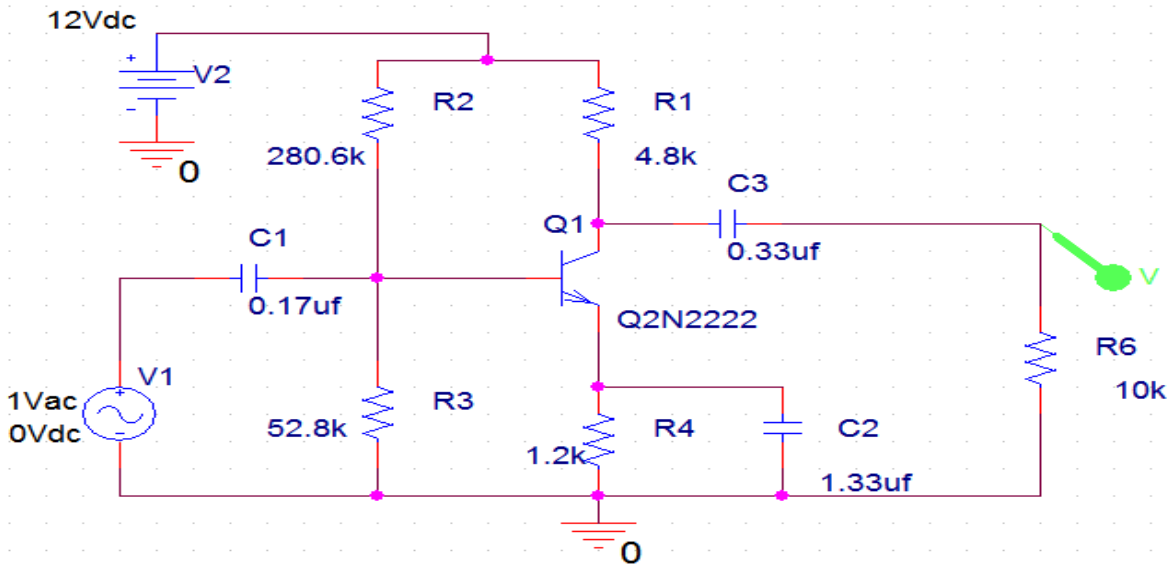
AIM:

To Design and Construct a Common Emitter **A**mplifier using Pspice simulation tool and to determine its: (a)Gain of the amplifier (b) Bandwidth of the amplifier

APPARATUS REQUIRED:

S.no	Requirements	Quantity
1	PC	1
2	Pspice Software	-

CIRCUITDIAGRAM:



PROCEDURE:

1. Click on the start menu and select the pspice simulation software
2. Select the parts required for the circuit from the parts menu and place them in the work space
3. Connect the parts using wires
4. Save the file and select the appropriate analysis
5. Simulate the circuit and observe the corresponding output waveforms

Simulated Output:

RESULT:

The Common Emitter Amplifier was simulated and the following results were determined 1.Gain of the amplifier : 2.Bandwidth of the Amplifier:

EXPT NO:09 **DATE:**

COMMON SOURCE AMPLIFIER

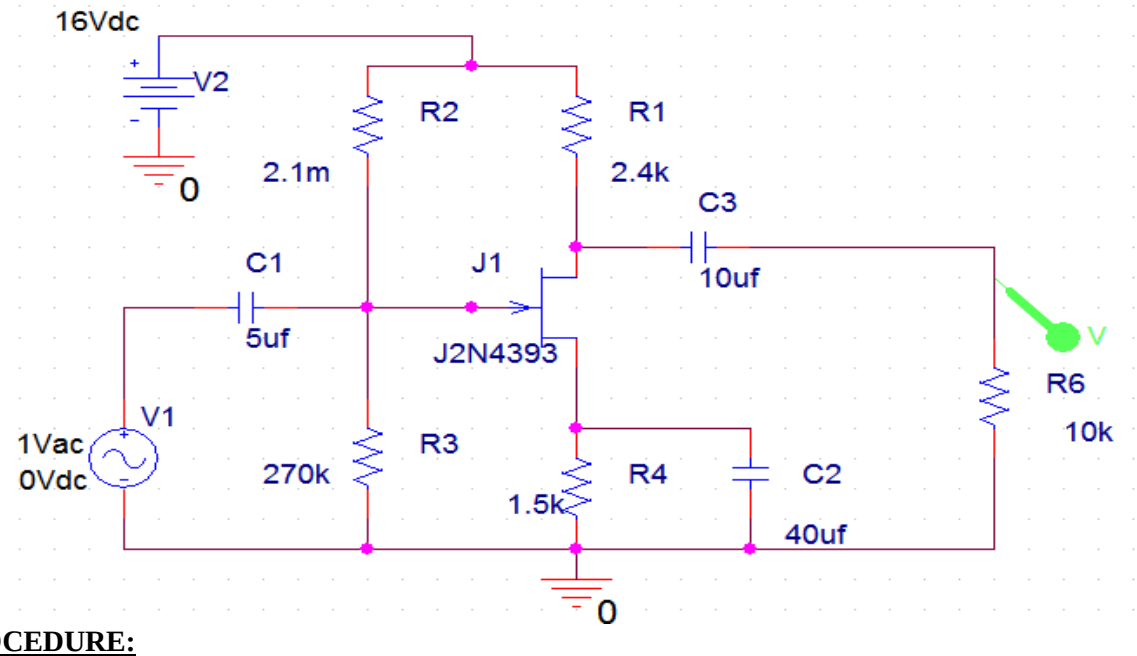
AIM:

To Design and Construct a Common Source **A**mplifier using Pspice simulation tool and to determine its: (a)Gain of the amplifier (b) Bandwidth of the amplifier

Apparatus Required:

S.no	Requirements	Quantity
1	PC	1
2	Pspice Software	-

CIRCUITDIAGRAM:



PROCEDURE:

1. Click on the start menu and select the pspice simulation software
2. Select the parts required for the circuit from the parts menu and place them in the work space
3. Connect the parts using wires
4. Save the file and select the appropriate analysis
5. Simulate the circuit and observe the corresponding output waveforms

Simulated Output:

RESULT:

The Common Source amplifier was simulated and the following results were determined 1.Gain of the amplifier : 2.Bandwidth of the Amplifier:

CASCADE AMPLIFIER

EXPERIMENT:10 **DATE:**

1. **OBJECTIVE:**

To Design and Construct a Cascaded **A**mplifier using Pspice simulation tool and to determine its:

a. Gain of the amplifier
b. Bandwidth of the amplifier
c. Gain -Bandwidth Product

2. **REQUIREMENTS:**

S. NO	Requirements	Quantity
1	PC	1
2	PSPICE Software	-

3. **THEORY:**

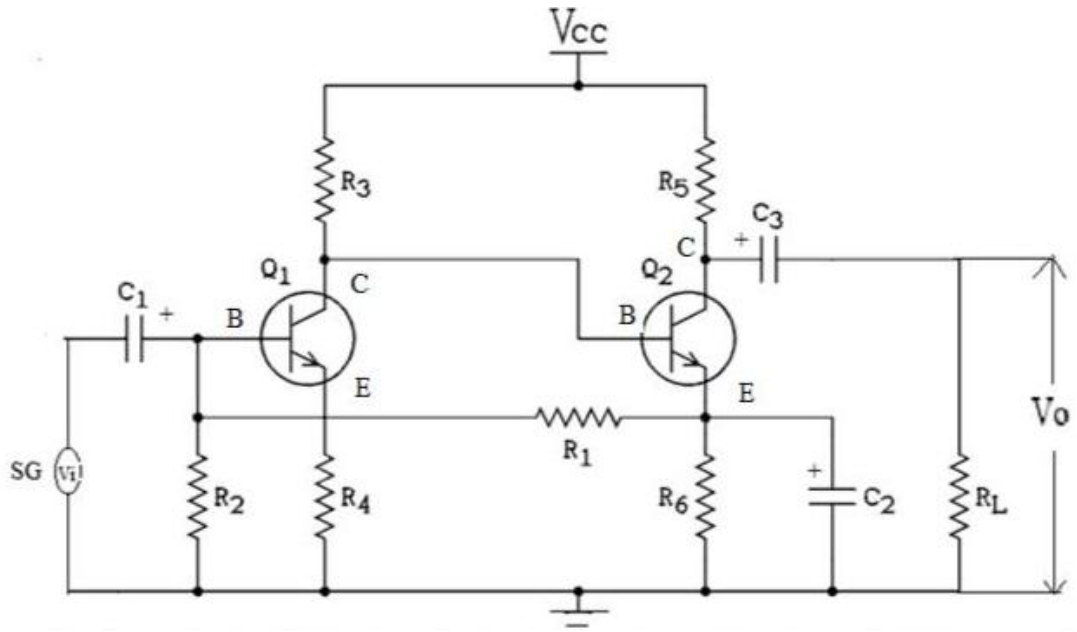
A cascade is type of multistage amplifier where two or more single stage amplifiers are connected serially. Many times the primary requirement of the amplifier cannot be achieved with single stage amplifier, because Of the limitation of the transistor parameters. In such situations more than one amplifier stages are cascaded such that input and output stages provide impedance matching requirements with some amplification and remaining middle stages provide most of the amplification. These types of amplifier circuits are employed in designing microphone and loudspeaker.

4. **PROCEDURE:**

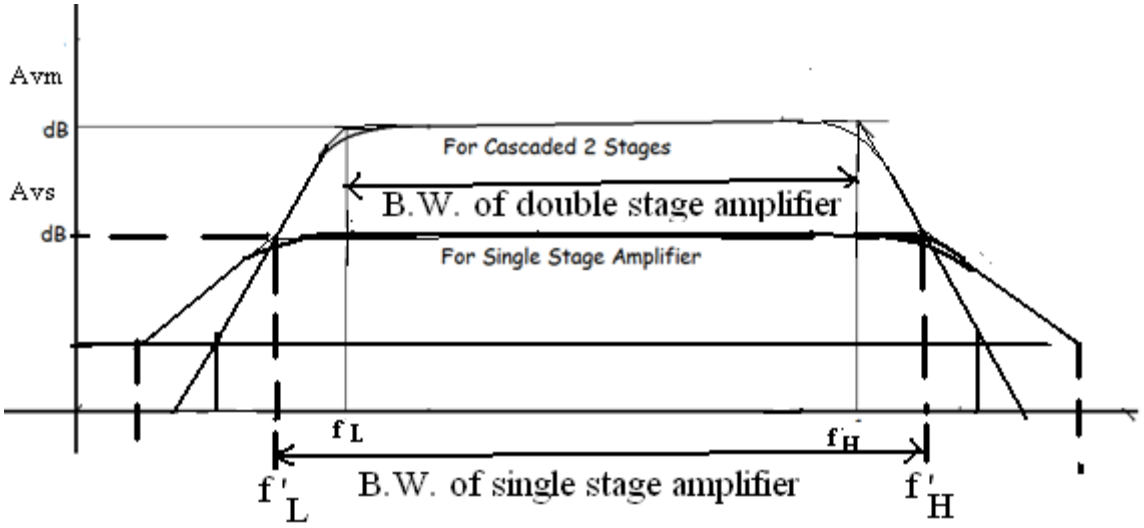
1. Click on the start menu and select the pspice simulation software
2. Select the parts required for the circuit from the parts menu and place them in the work space
3. Connect the parts using wires
4. Save the file and select the appropriate analysis

5. Simulate the circuit and observe the corresponding output waveforms

CIRCUIT DIAGRAM OF MULTISTAGE AMPLIFIER



Model Graph:



5. RESULT:

INFERENCE:

The Common Emitter Amplifier was simulated and the following results were determined:

a) Gain of the amplifier :

b) Bandwidth of the amplifier :

c) Gain-Bandwidth product :

DIGITAL EXPERIMENTS

STUDY OF LOGIC GATES

AIM:

To study about logic gates and verify their truth tables.

COMPONENTS AND EQUIPMENTS REQUIRED:

SL No.	COMPONENT	SPECIFICATION	QTY
1.	AND GATE	IC 7408	1
2.	OR GATE	IC 7432	1
3.	NOT GATE	IC 7404	1
4.	NAND GATE 2 I/P	IC 7400	1
5.	NOR GATE	IC 7402	1
6.	X-OR GATE	IC 7486	1

7.	NAND GATE 3 I/P	IC 7410	1
8.	IC TRAINER KIT	-	1
9.	PATCH CORD	-	14

THEORY:

Circuit that takes the logical decision and the process are called logic gates. Each gate has one or more input and only one output.

OR, AND and NOT are basic gates. NAND, NOR and X-OR are known as universal gates. Basic gates form these gates.

AND GATE:

The AND gate performs a logical multiplication commonly known as AND function. The output is high when both the inputs are high. The output is low level when any one of the inputs is low.

OR GATE:

The OR gate performs a logical addition commonly known as OR function. The output is high when any one of the inputs is high. The output is low level when both the inputs are low.

NOT GATE:

The NOT gate is called an inverter. The output is high when the input is low. The output is low when the input is high.

NAND GATE:

The NAND gate is a contraction of AND-NOT. The output is high when both inputs are low and any one of the input is low .The output is low level when both inputs are high.

NOR GATE:

The NOR gate is a contraction of OR-NOT. The output is high when both inputs are low. The output is low when one or both inputs are high.

X-OR GATE:

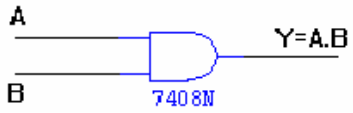
The output is high when any one of the inputs is high. The output is low when both the inputs are low and both the inputs are high.

PROCEDURE:

(i) Connections are given as per circuit diagram.
(ii) Logical inputs are given as per circuit diagram.
(iii) Observe the output and verify the truth table.

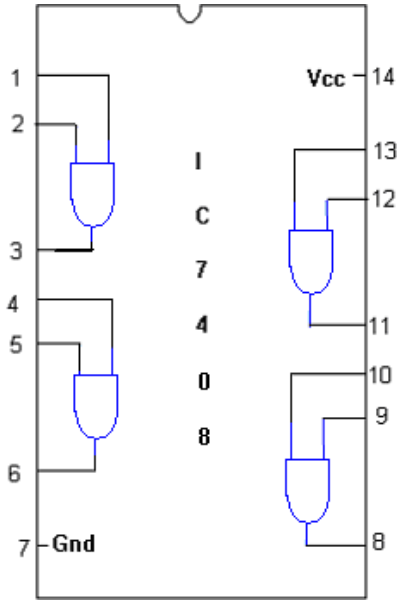
AND GATE:

SYMBOL: **PIN DIAGRAM:**



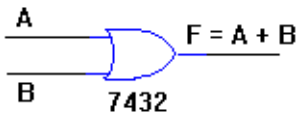
TRUTH TABLE

A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

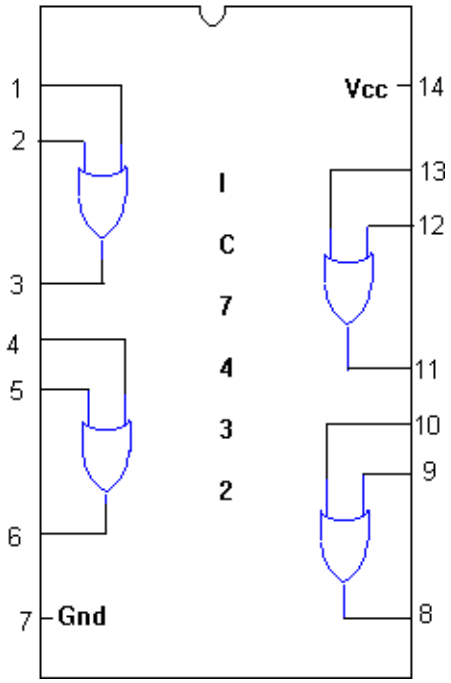


OR GATE:

SYMBOL :



PIN DIAGRAM :



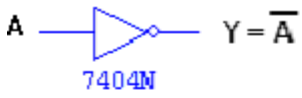
TRUTH TABLE

A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

NOT GATE:

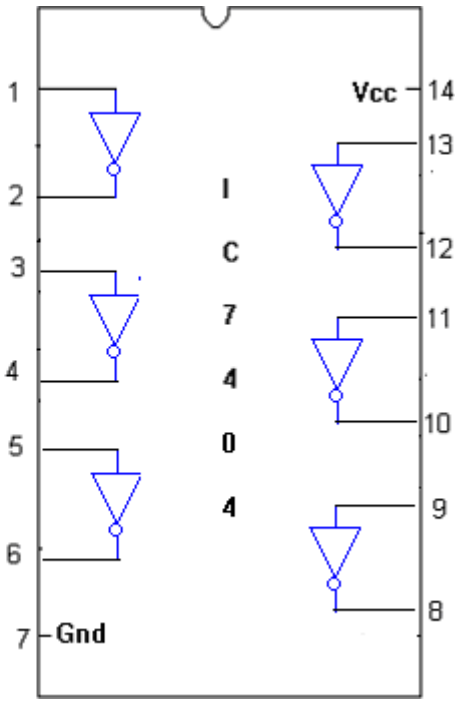
SYMBOL:

PIN DIAGRAM:



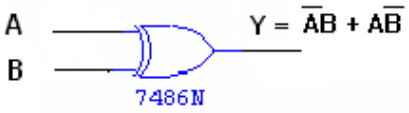
TRUTH TABLE :

A	$\overline{A}$
0	1
1	0



X-OR GATE :

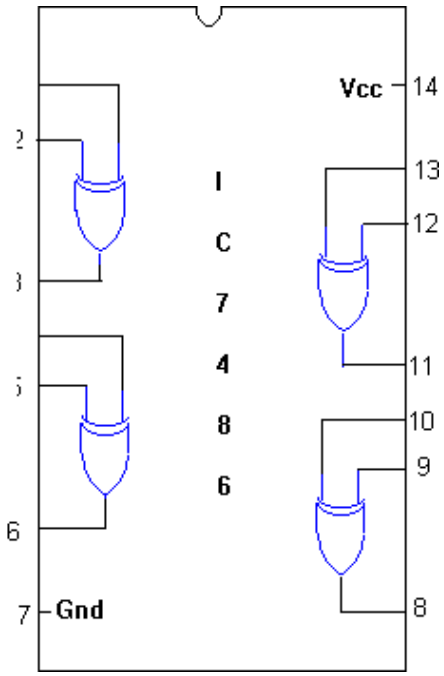
SYMBOL :



TRUTH TABLE :

A	B	$\overline{A}B + A\overline{B}$
0	0	0
0	1	1
1	0	1
1	1	0

PIN DIAGRAM :



2-INPUT NAND GATE:

SYMBOL:

PIN DIAGRAM:

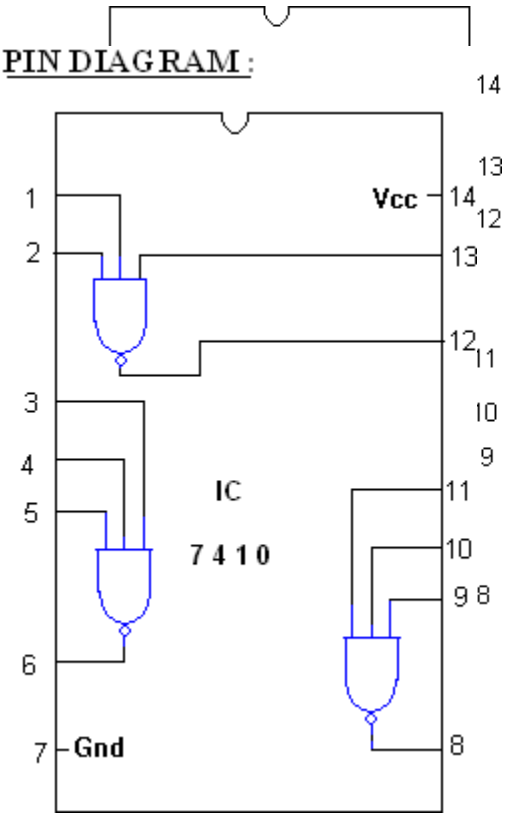
INPUT NAND GATE :

SYMBOL :

TRUTH TABLE

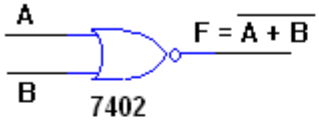
A	B	C	$\overline{A.B.C}$
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

PIN DIAGRAM :



NOR GATE:

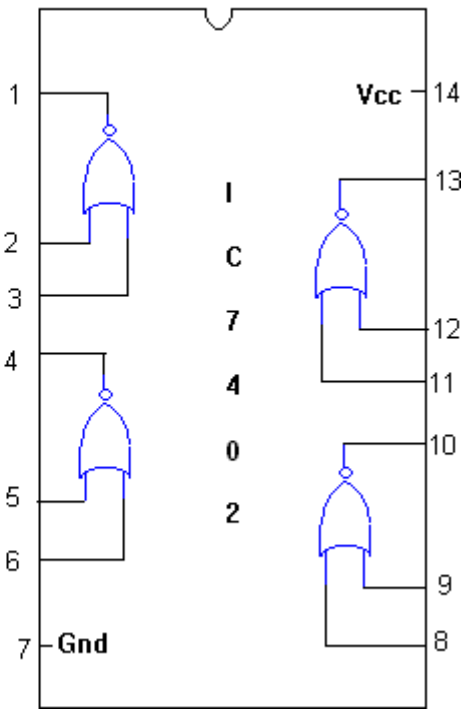
SYMBOL :



TRUTH TABLE

A	B	$\overline{A+B}$
0	0	1
0	1	1
1	0	1
1	1	0

PIN DIAGRAM :



RESULT:

The Logic gates have been studied and their truth table has been verified.

DESIGN AND IMPLEMENTATION OF CODE CONVERTOR

EXPERIMENT:11 **DATE:**

AIM:

To design and implement 4-bit

(i) Binary to gray code converter
(ii) Gray to binary code converter
(iii) BCD to excess-3 code converter
(iv) Excess-3 to BCD code converter

COMPONENTS AND EQUIPMENTS REQUIRED:

Sl.No.	COMPONENT	SPECIFICATION	QTY.
1.	X-OR GATE	IC 7486	1
2.	AND GATE	IC 7408	1
3.	OR GATE	IC 7432	1
4.	NOT GATE	IC 7404	1
5.	IC TRAINER KIT	-	1
6.	PATCH CORDS	-	35

THEORY:

The availability of large variety of codes for the same discrete elements of information results in the use of different codes by different systems. A conversion circuit must be inserted between the two systems if each uses different codes for same information. Thus, code converter is a circuit that makes the two systems compatible even though each uses different binary code.

The bit combination assigned to binary code to gray code. Since each code uses four bits to represent a decimal digit. There are four inputs and four outputs. Gray code is a non-weighted code.

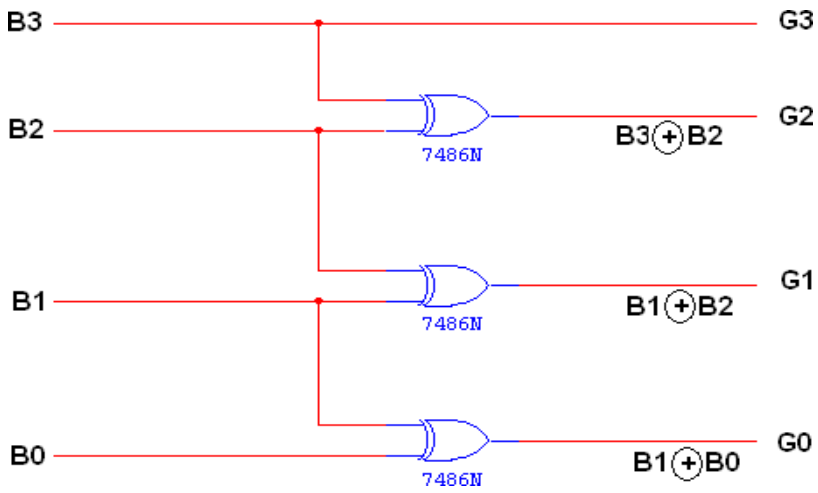
The input variable are designated as B3, B2, B1, B0 and the output variables are designated as C3, C2, C1, Co. from the truth table, combinational circuit is designed. The Boolean functions are obtained from K-Map for each output variable.

A code converter is a circuit that makes the two systems compatible even though each uses a different binary code. To convert from binary code to Excess-3 code, the input lines must supply the bit combination of elements as specified by code and the output lines generate the corresponding bit combination of code. Each one of the four maps represents one of the four outputs of the circuit as a function of the four input variables.

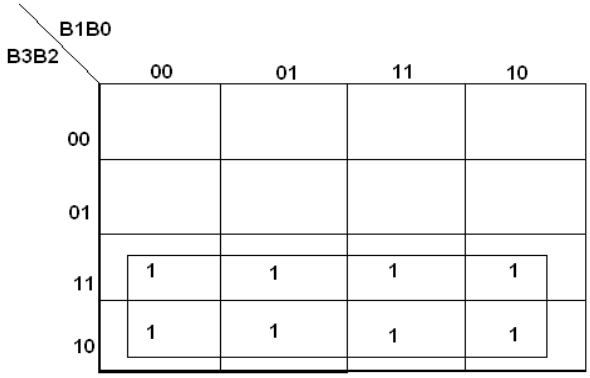
A two-level logic diagram may be obtained directly from the Boolean expressions derived by the maps. These are various other possibilities for a logic diagram that implements this circuit. Now the OR gate whose output is C+D has been used to implement partially each of three outputs.

LOGIC DIAGRAM:

BINARY TO GRAY CODE CONVERTOR

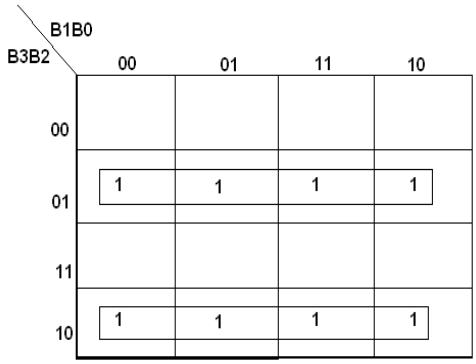


K-Map for G_3:



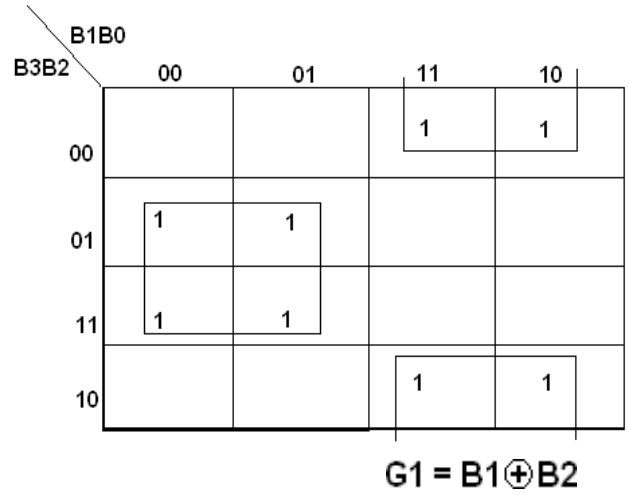
$G_3 = B_3$

K-Map for G_2:

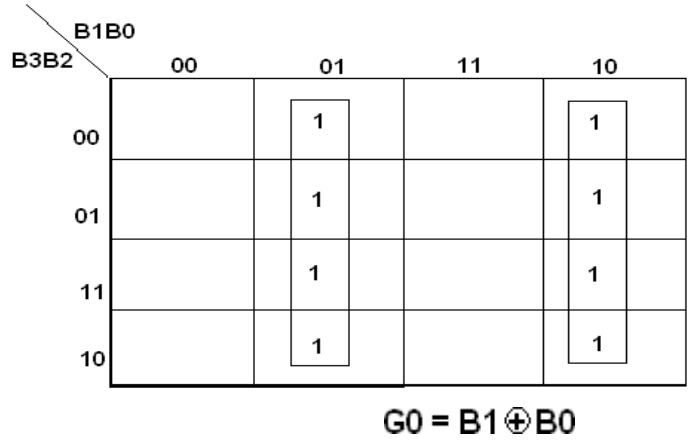


G2 = B3⊕B2

K-Map for G_1:



K-Map for G_0:

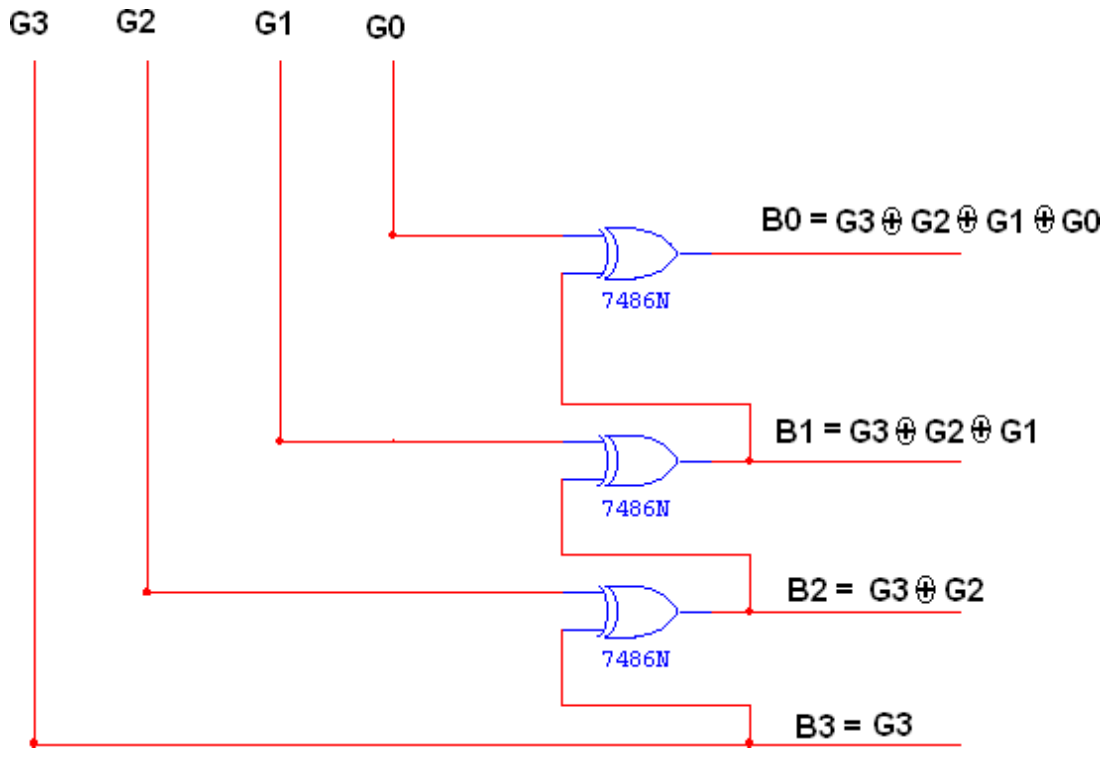


TRUTH TABLE:

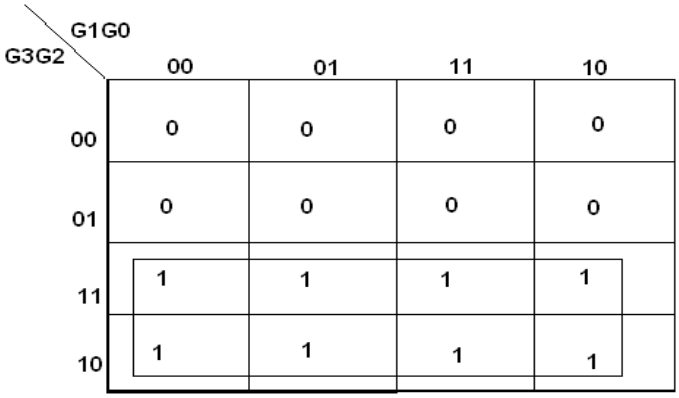
Binary input				Gray code output			
B3	**B2**	**B1**	**B0**	**G3**	**G2**	**G1**	**G0**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
0	**0**	**0**	**1**	**0**	**0**	**0**	**1**
0	**0**	**1**	**0**	**0**	**0**	**1**	**1**
0	**0**	**1**	**1**	**0**	**0**	**1**	**0**
0	**1**	**0**	**0**	**0**	**1**	**1**	**0**
0	**1**	**0**	**1**	**0**	**1**	**1**	**1**
0	**1**	**1**	**0**	**0**	**1**	**0**	**1**
0	**1**	**1**	**1**	**0**	**1**	**0**	**0**
1	**0**	**0**	**0**	**1**	**1**	**0**	**0**
1	**0**	**0**	**1**	**1**	**1**	**0**	**1**
1	**0**	**1**	**0**	**1**	**1**	**1**	**1**
1	**0**	**1**	**1**	**1**	**1**	**1**	**0**
1	**1**	**0**	**0**	**1**	**0**	**1**	**0**
1	**1**	**0**	**1**	**1**	**0**	**1**	**1**
1	**1**	**1**	**0**	**1**	**0**	**0**	**1**
1	**1**	**1**	**1**	**1**	**0**	**0**	**0**

LOGIC DIAGRAM:

GRAY CODE TO BINARY CONVERTOR

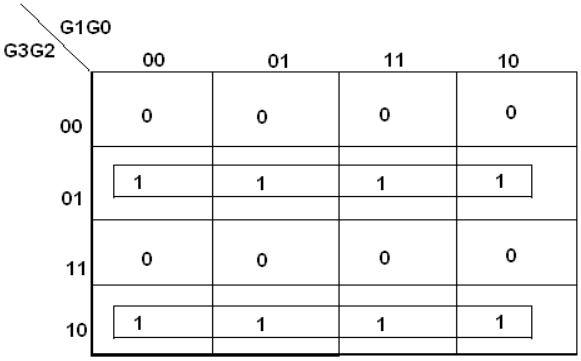


K-Map for B_3:



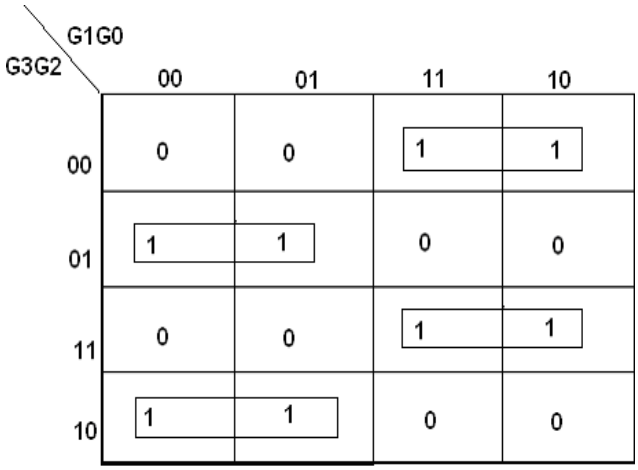
B3 = G3

K-Map for B_2:



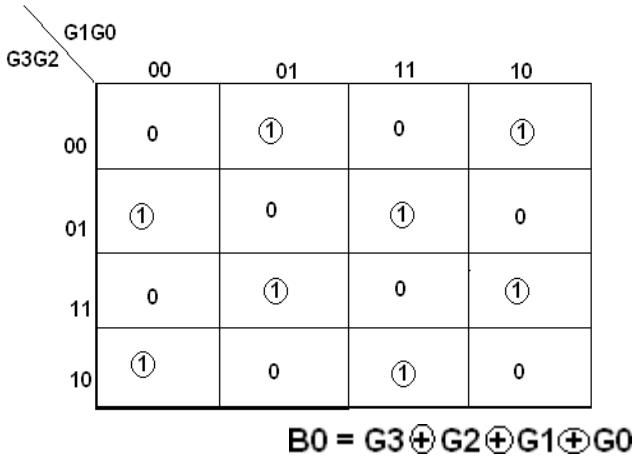
B2 = G3⊕G2

K-Map for B_1:



B1 = G3⊕G2⊕G1

K-Map for B_0:

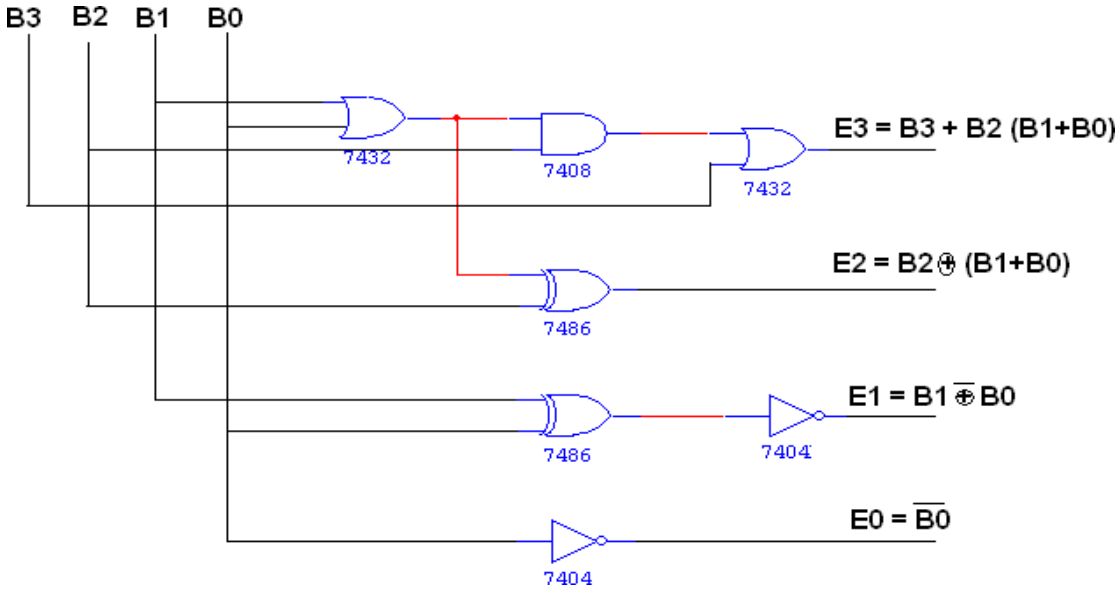


TRUTH TABLE:

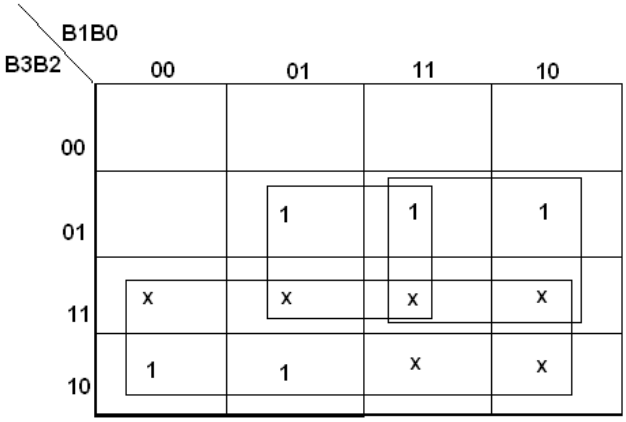
Gray Code				Binary Code			
G3	**G2**	**G1**	**G0**	**B3**	**B2**	**B1**	**B0**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
0	**0**	**0**	**1**	**0**	**0**	**0**	**1**
0	**0**	**1**	**1**	**0**	**0**	**1**	**0**
0	**0**	**1**	**0**	**0**	**0**	**1**	**1**
0	**1**	**1**	**0**	**0**	**1**	**0**	**0**
0	**1**	**1**	**1**	**0**	**1**	**0**	**1**
0	**1**	**0**	**1**	**0**	**1**	**1**	**0**
0	**1**	**0**	**0**	**0**	**1**	**1**	**1**
1	**1**	**0**	**0**	**1**	**0**	**0**	**0**
1	**1**	**0**	**1**	**1**	**0**	**0**	**1**
1	**1**	**1**	**1**	**1**	**0**	**1**	**0**
1	**1**	**1**	**0**	**1**	**0**	**1**	**1**
1	**0**	**1**	**0**	**1**	**1**	**0**	**0**
1	**0**	**1**	**1**	**1**	**1**	**0**	**1**
1	**0**	**0**	**1**	**1**	**1**	**1**	**0**
1	**0**	**0**	**0**	**1**	**1**	**1**	**1**

LOGIC DIAGRAM:

BCD TO EXCESS-3 CONVERTOR

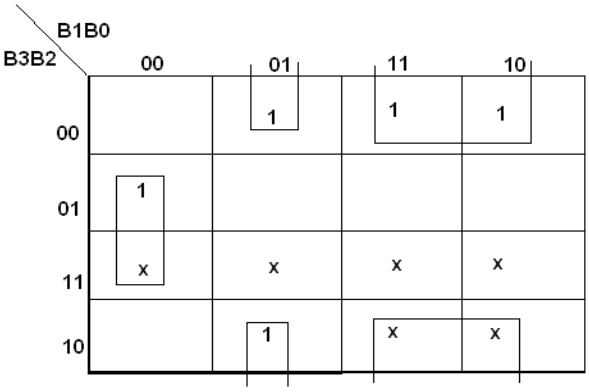


K-Map for E_3:



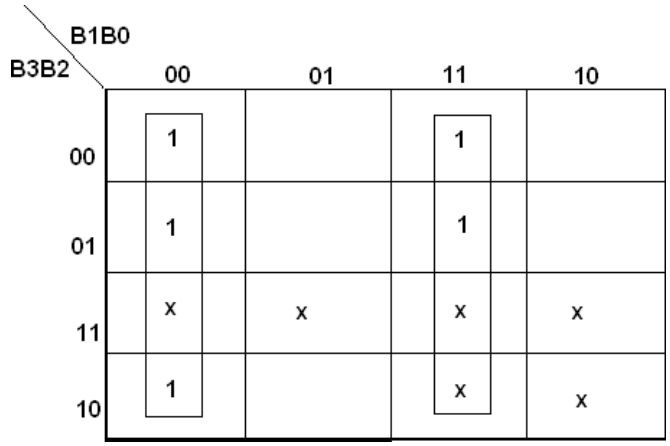
E3 = B3 + B2 (B0 + B1)

K-Map for E_2:



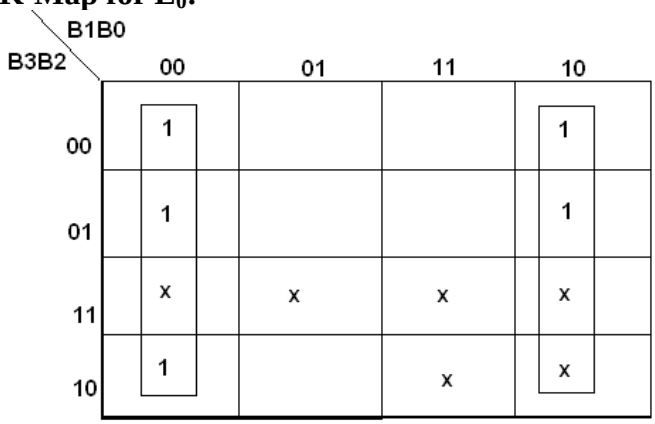
E2 = B2⊕ (B1 + B0)

K-Map for E_1:



$E1 = B1 \bar{\oplus} B0$

K-Map for E_0:



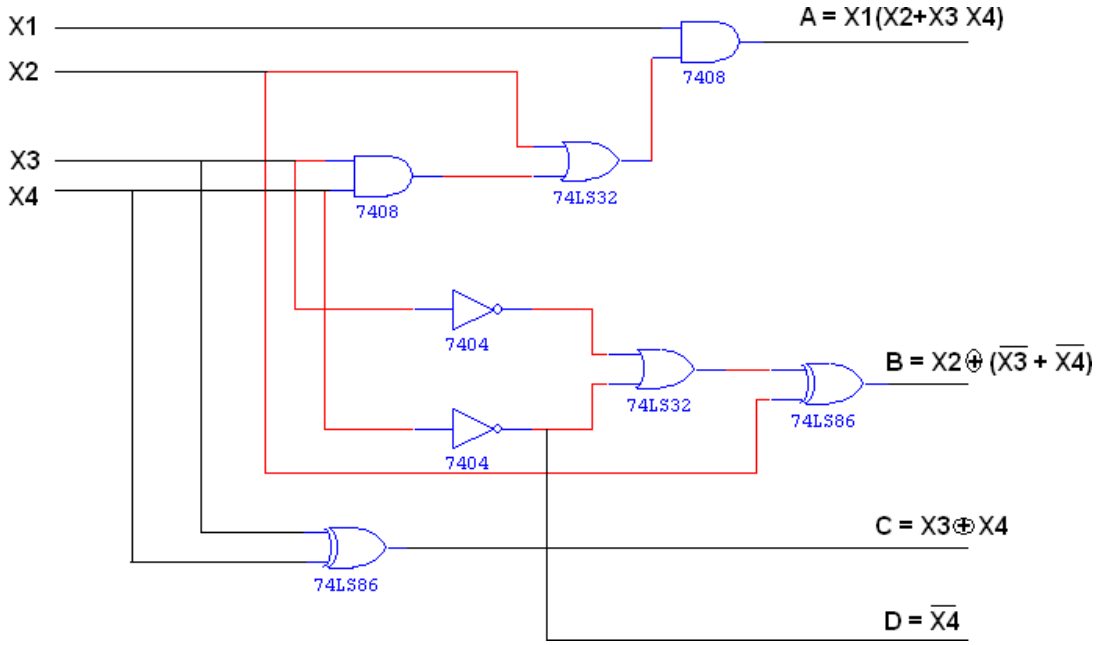
$E0 = \overline{B0}$

TRUTH TABLE:

BCD input				Excess – 3 output			
B3	**B2**	**B1**	**B0**	**G3**	**G2**	**G1**	**G0**
0	**0**	**0**	**0**	**0**	**0**	**1**	**1**
0	**0**	**0**	**1**	**0**	**1**	**0**	**0**
0	**0**	**1**	**0**	**0**	**1**	**0**	**1**
0	**0**	**1**	**1**	**0**	**1**	**1**	**0**
0	**1**	**0**	**0**	**0**	**1**	**1**	**1**
0	**1**	**0**	**1**	**1**	**0**	**0**	**0**
0	**1**	**1**	**0**	**1**	**0**	**0**	**1**
0	**1**	**1**	**1**	**1**	**0**	**1**	**0**
1	**0**	**0**	**0**	**1**	**0**	**1**	**1**
1	**0**	**0**	**1**	**1**	**1**	**0**	**0**
1	**0**	**1**	**0**	**x**	**x**	**x**	**x**
1	**0**	**1**	**1**	**x**	**x**	**x**	**x**
1	**1**	**0**	**0**	**x**	**x**	**x**	**x**
1	**1**	**0**	**1**	**x**	**x**	**x**	**x**
1	**1**	**1**	**0**	**x**	**x**	**x**	**x**
1	**1**	**1**	**1**	**x**	**x**	**x**	**x**

LOGIC DIAGRAM:

EXCESS-3 TO BCD CONVERTOR



K-Map for A:

X1 X2 \ X3 X4	00	01	11	10
00	X	X	0	X
01	0	0	0	0
11	1	X	X	X
10	0	0	1	0

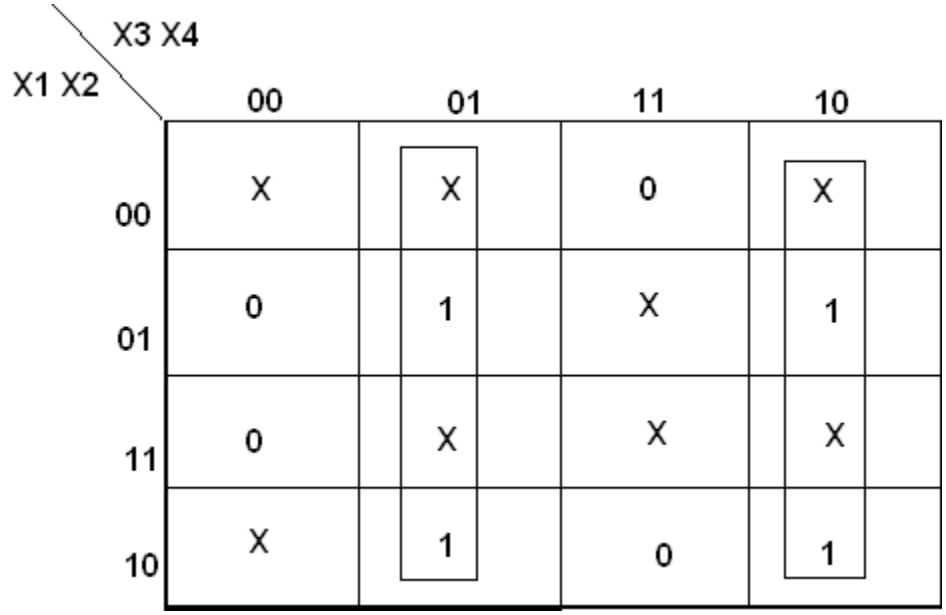
A = X1 X2 + X3 X4 X1

K-Map for B:

X1 X2 \ X3 X4	00	01	11	10
00	X	X	0	X
01	0	0	1	0
11	0	X	X	X
10	1	1	0	1

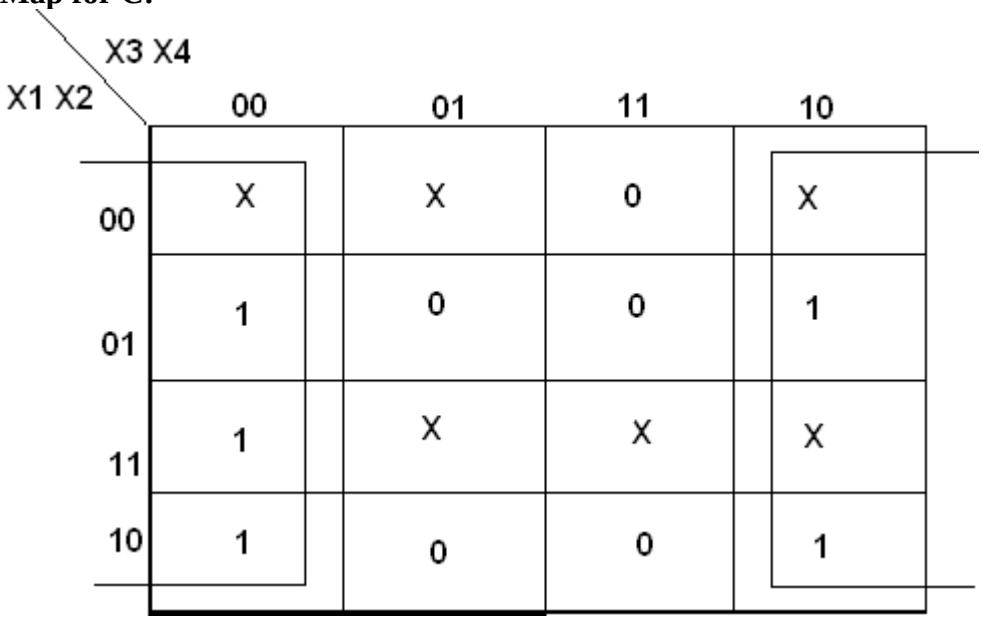
B = X2⊕(X3 + X4)

K-Map for C:



$C = X3 \oplus X4$

K-Map for C:



$D = \overline{X4}$

TRUTH TABLE:

| **Excess – 3 Input** | **BCD Output** |

B3	B2	B1	B0	G3	G2	G1	G0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	1
0	1	0	1	0	0	1	0
0	1	1	0	0	0	1	1
0	1	1	1	0	1	0	0
1	0	0	0	0	1	0	1
1	0	0	1	0	1	1	0
1	0	1	0	0	1	1	1
1	0	1	1	1	0	0	0
1	1	0	0	1	0	0	1

PROCEDURE:

(i) Connections were given as per circuit diagram.
(ii) Logical inputs were given as per truth table
(iii) Observe the logical output and verify with the truth tables.

RESULT:

Hence designed and implemented 4-bit
(i) Binary to gray code converter
(ii) Gray to binary code converter
(iii) BCD to excess-3 code converter
(iv) Excess-3 to BCD code converter

DESIGN OF 4-BIT ADDER AND SUBTRACTOR

EXPERIMENT:12 **DATE:**

AIM:

To design and implement 4-bit adder and subtractor using IC 7483.

COMPONENTS AND EQUIPMENTS REQUIRED:

Sl.No.	COMPONENT	SPECIFICATION	QTY.
1.	IC	IC 7483	1
2.	EX-OR GATE	IC 7486	1
3.	NOT GATE	IC 7404	1
3.	IC TRAINER KIT	-	1
4.	PATCH CORDS	-	40

THEORY:

4 BIT BINARY ADDER:

A binary adder is a digital circuit that produces the arithmetic sum of two binary numbers. It can be constructed with full adders connected in cascade, with the output carry from each full adder connected to the input carry of next full adder in chain. The augends bits of 'A' and the addend bits of 'B' are designated by subscript numbers from right to left, with subscript 0 denoting the least significant bits. The carries are connected in chain through the full adder. The input carry to the adder is C_0 and it ripples through the full adder to the output carry C_4.

4 BIT BINARY SUBTRACTOR:

The circuit for subtracting A-B consists of an adder with inverters, placed between each data input 'B' and the corresponding input of full adder. The input carry C_0 must be equal to 1 when performing subtraction.

4 BIT BINARY ADDER/SUBTRACTOR:

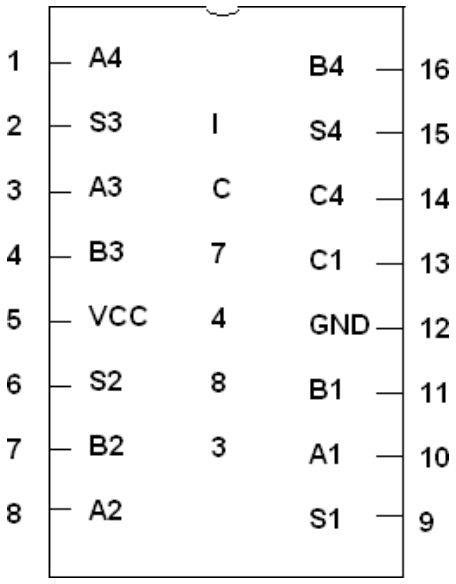
The addition and subtraction operation can be combined into one circuit with one common binary adder. The mode input M controls the operation. When M=0, the circuit is adder circuit. When M=1, it becomes subtractor.

4 BIT BCD ADDER:

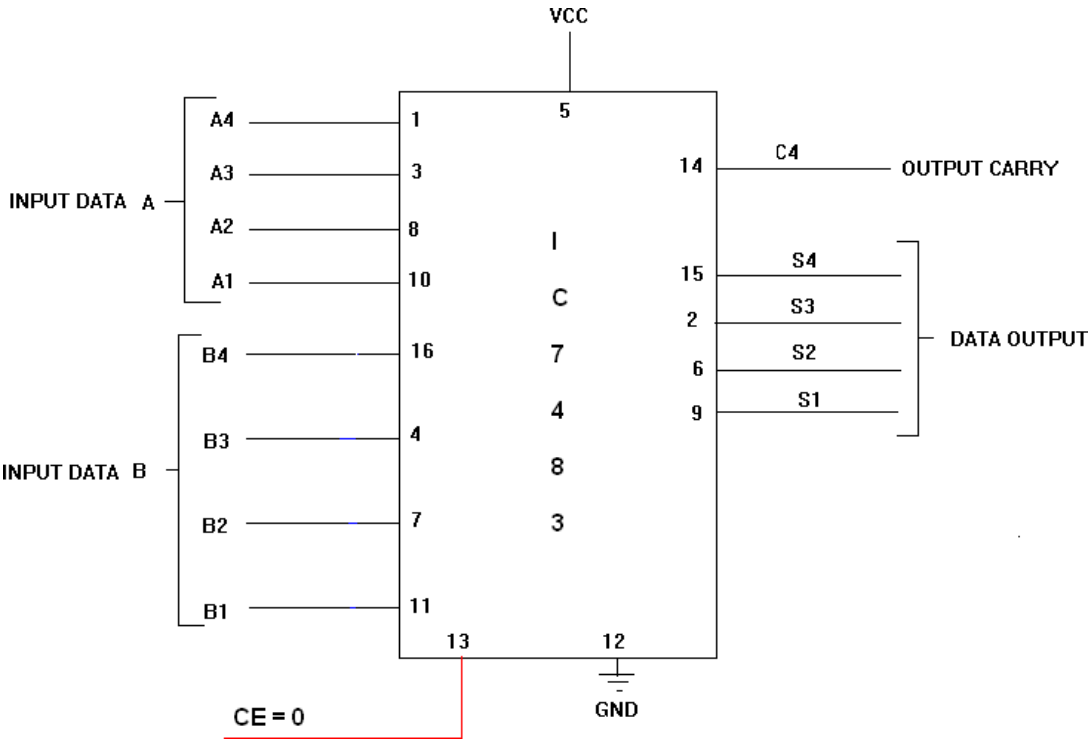
Consider the arithmetic addition of two decimal digits in BCD, together with an input carry from a previous stage. Since each input digit does not exceed 9, the output sum cannot be greater than 19, the 1 in the sum being an input carry. The output of two decimal digits must be represented in BCD and should appear in the form listed in the columns.

ABCD adder that adds 2 BCD digits and produce a sum digit in BCD. The 2 decimal digits, together with the input carry, are first added in the top 4 bit adder to produce the binary sum.

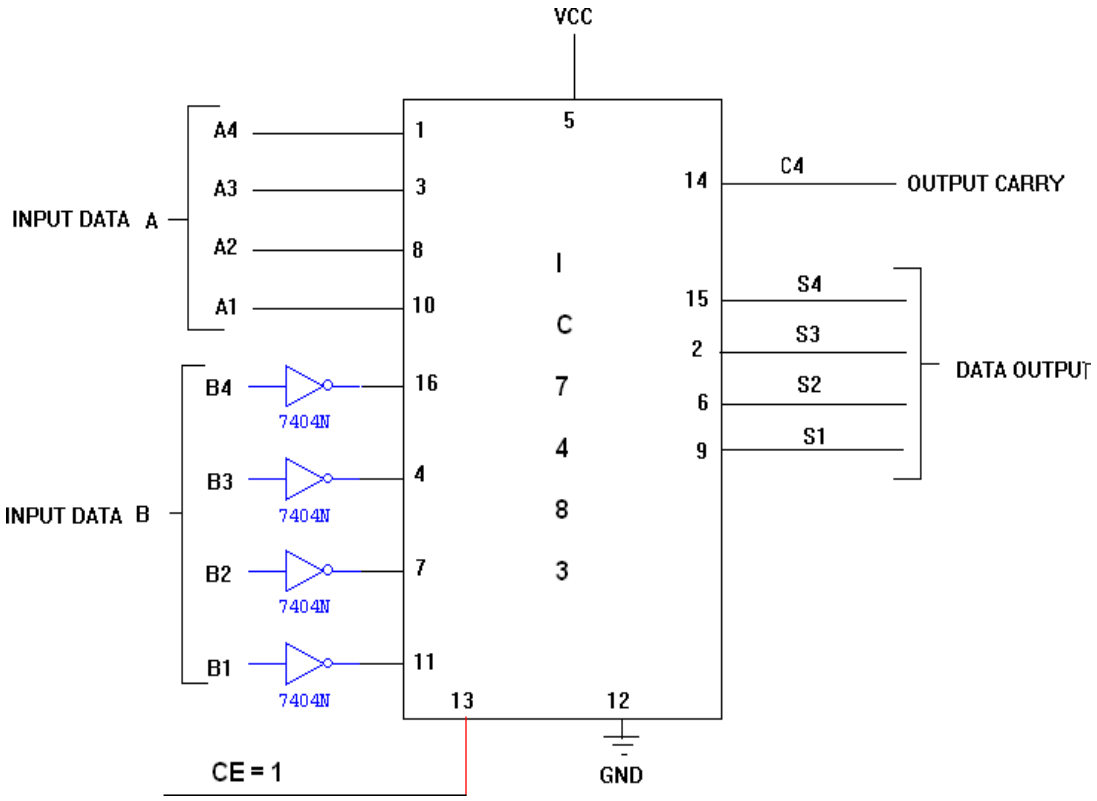
PIN DIAGRAM FOR IC 7483:



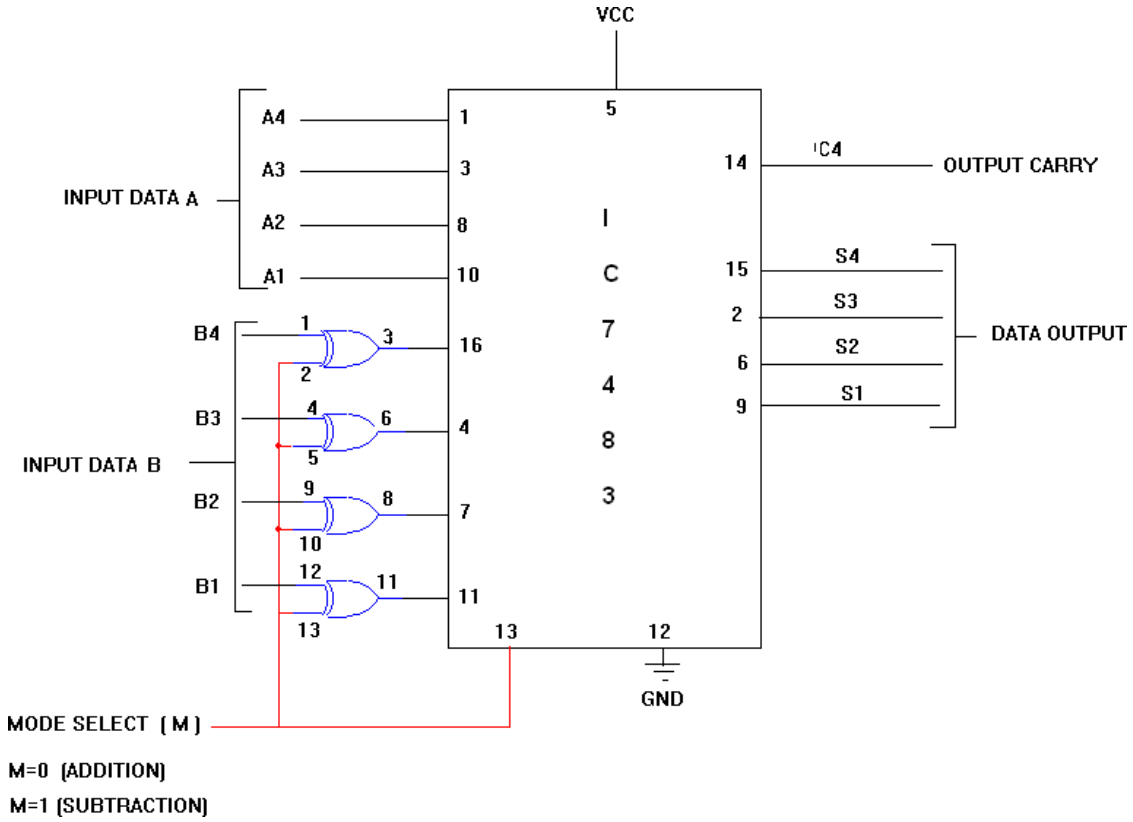
LOGIC DIAGRAM:
3-BIT BINARY ADDER



LOGIC DIAGRAM:
4-BIT BINARY SUBTRACTOR



LOGIC DIAGRAM:
4-BIT BINARY ADDER/SUBTRACTOR



TRUTH TABLE:

Input Data A				Input Data B				Addition					Subtraction				
A4	A3	A2	A1	B4	B3	B2	B1	C	S4	S3	S2	S1	B	D4	D3	D2	D1
1	0	0	0	0	0	1	0	0	1	0	1	0	1	0	1	1	0
1	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	0
0	0	1	0	1	0	0	0	0	1	0	1	0	0	1	0	1	0
0	0	0	1	0	1	1	1	0	1	0	0	0	0	1	0	1	0
1	0	1	0	1	0	1	1	1	0	0	1	0	0	1	1	1	1
1	1	1	0	1	1	1	1	1	1	0	1	0	0	1	1	1	1
1	0	1	0	1	1	0	1	1	0	1	1	1	0	1	1	0	1

PROCEDURE:

(i) Connections were given as per circuit diagram.
(ii) Logical inputs were given as per truth table
(iii) Observe the logical output and verify with the truth tables.

RESULT:

Hence designed and implemented 4-bit adder and subtractor using IC 7483

DESIGN AND IMPLEMENTATION OF MULTIPLEXER AND DEMULTIPLEXER

EXPERIMENT:13 **DATE:**

AIM:

To design and implement multiplexer and demultiplexer using logic gates and study of IC 74150 and IC 74154.

COMPONENTS AND EQUIPMENTS REQUIRED:

S.No.	COMPONENT	SPECIFICATION	QTY.
1.	3 I/P AND GATE	IC 7411	2
2.	OR GATE	IC 7432	1
3.	NOT GATE	IC 7404	1
2.	IC TRAINER KIT	-	1
3.	PATCH CORDS	-	32

THEORY:

MULTIPLEXER:

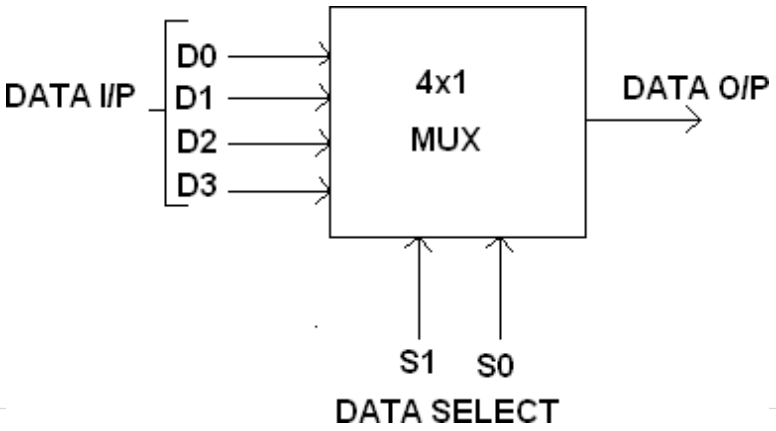
Multiplexer means transmitting a large number of information units over a smaller number of channels or lines. A digital multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line. The selection of a particular input line is controlled by a set of selection lines. Normally there are 2^n input line and n selection lines whose bit combination determine which input is selected.

DEMULTIPLEXER:

The function of Demultiplexer is in contrast to multiplexer function. It takes information from one line and distributes it to a given number of output lines. For this reason, the demultiplexer is also known as a data distributor. Decoder can also be used as demultiplexer.

In the 1: 4 demultiplexer circuit, the data input line goes to all of the AND gates. The data select lines enable only one gate at a time and the data on the data input line will pass through the selected gate to the associated data output line.

BLOCK DIAGRAM FOR 4:1 MULTIPLEXER:

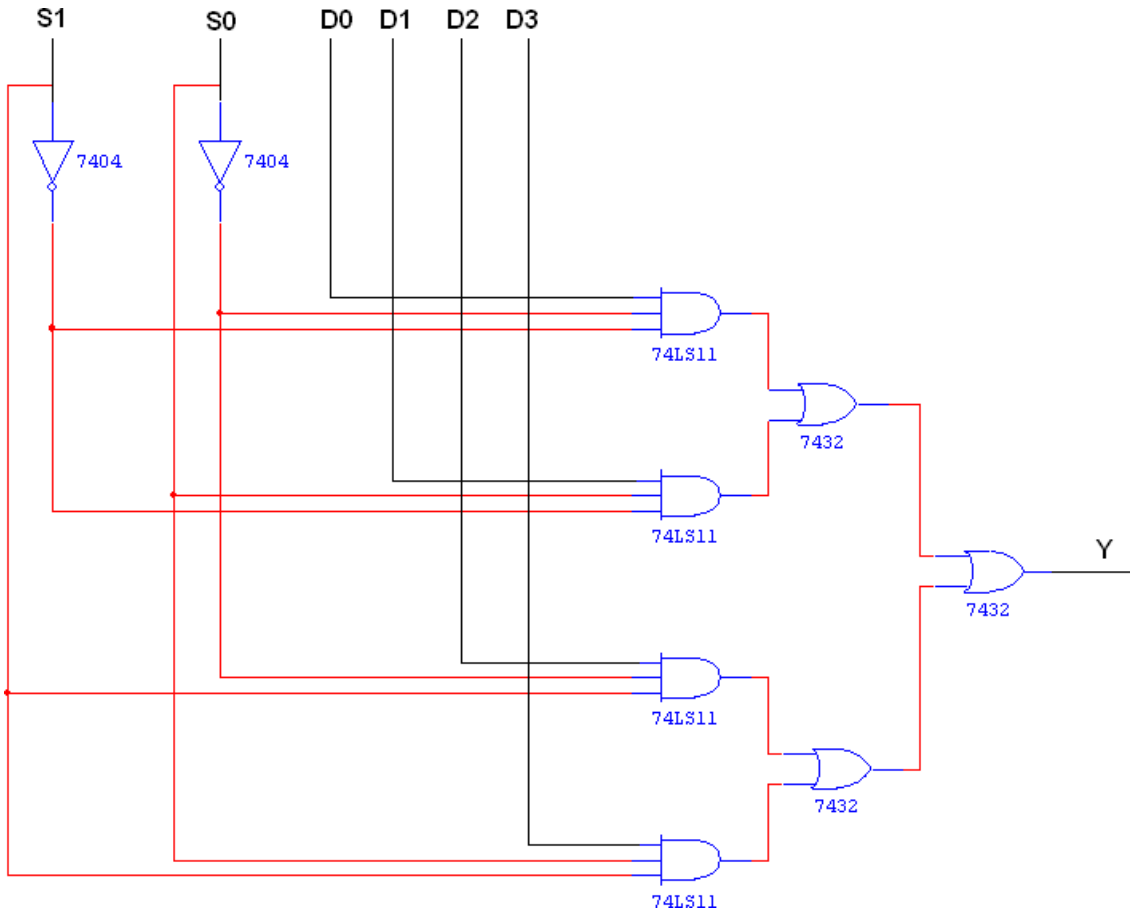


FUNCTION TABLE:

S1	S0	INPUTS Y
0	0	D0 → D0 S1' S0'
0	1	D1 → D1 S1' S0
1	0	D2 → D2 S1 S0'
1	1	D3 → D3 S1 S0

Y = D0 S1' S0' + D1 S1' S0 + D2 S1 S0' + D3 S1 S0

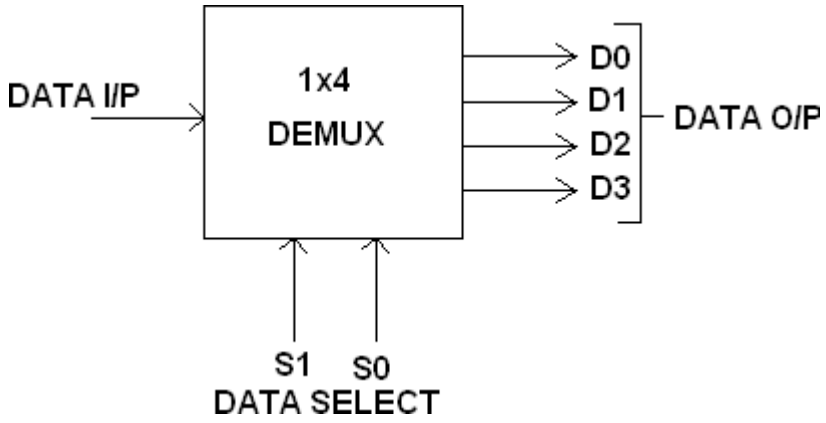
CIRCUIT DIAGRAM FOR MULTIPLEXER:



TRUTH TABLE:

S1	S0	Y = OUTPUT
0	0	D0
0	1	D1
1	0	D2
1	1	D3

BLOCK DIAGRAM FOR 1:4 DEMULTIPLEXERS:

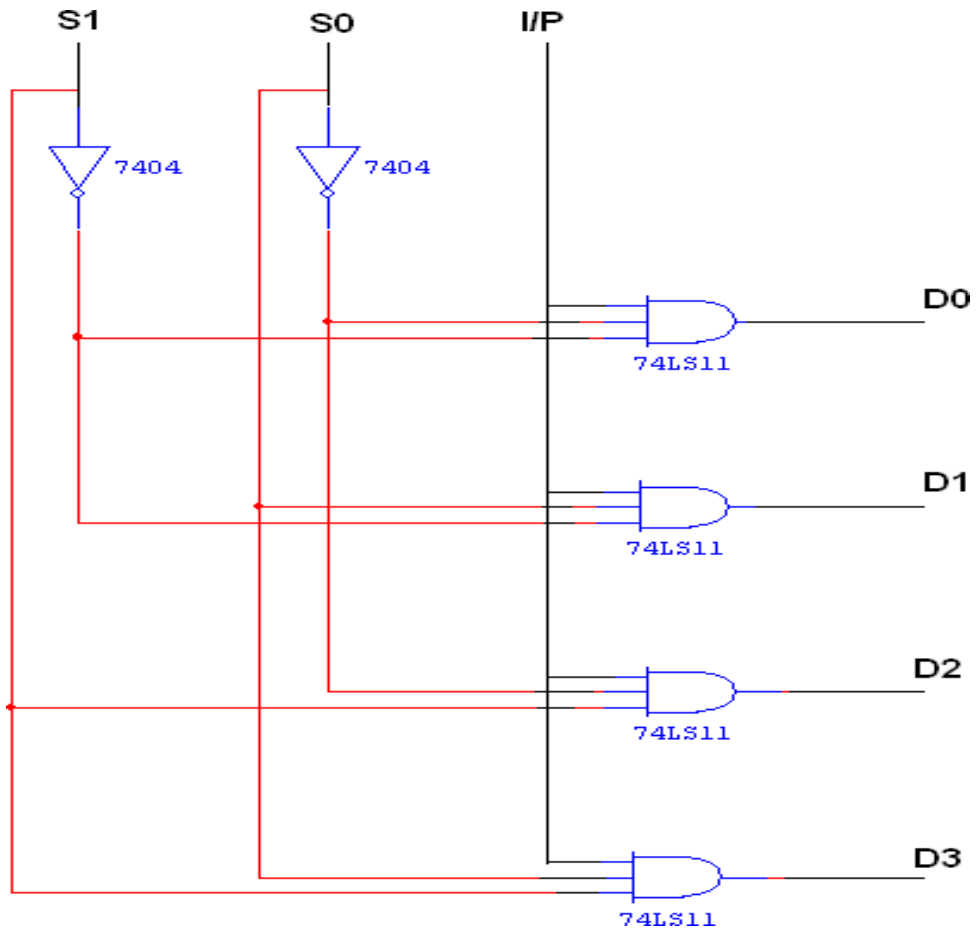


FUNCTION TABLE:

S1	S0	INPUT
0	0	X → D0 = X S1' S0'
0	1	X → D1 = X S1' S0
1	0	X → D2 = X S1 S0'
1	1	X → D3 = X S1 S0

Y = X S1' S0' + X S1' S0 + X S1 S0' + X S1 S0

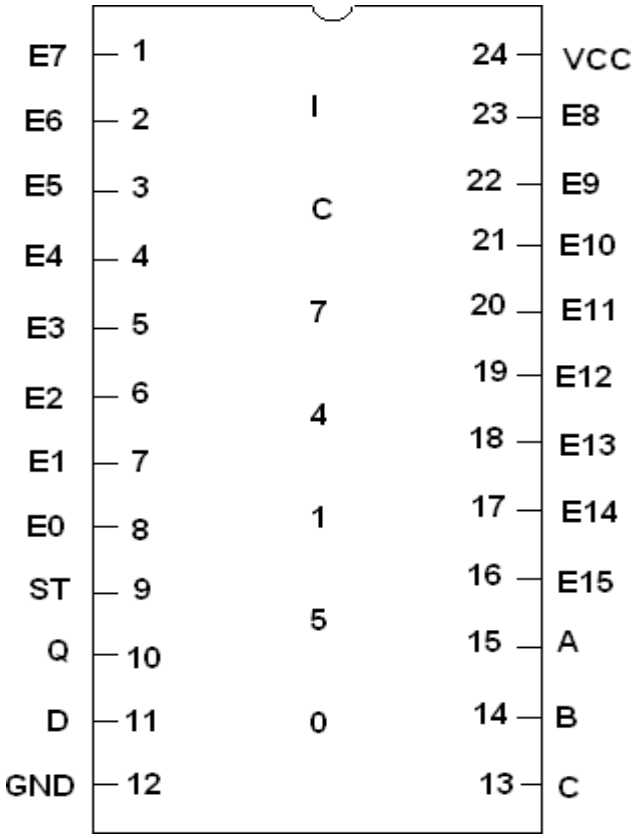
LOGIC DIAGRAM FOR DEMULTIPLEXER:



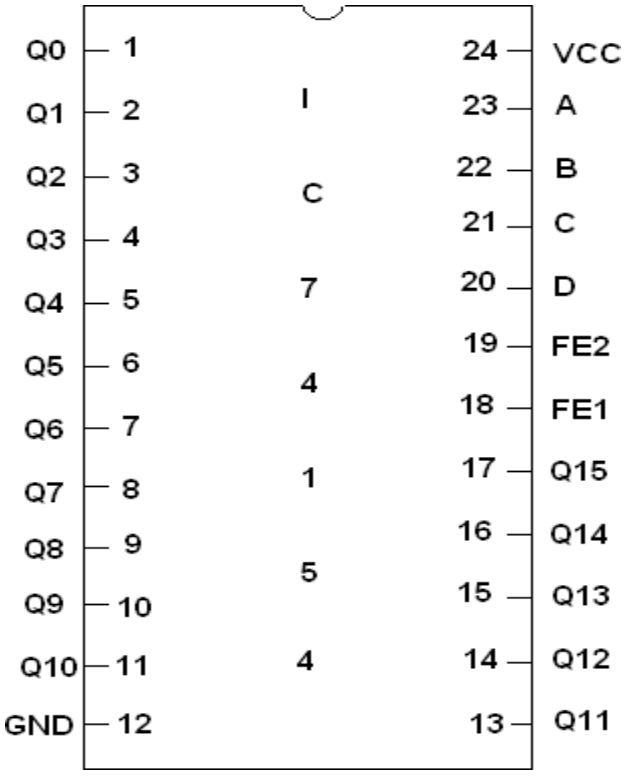
TRUTH TABLE:

INPUT			OUTPUT			
S1	**S0**	**I/P**	**D0**	**D1**	**D2**	**D3**
0	**0**	**0**	**0**	**0**	**0**	**0**
0	**0**	**1**	**1**	**0**	**0**	**0**
0	**1**	**0**	**0**	**0**	**0**	**0**
0	**1**	**1**	**0**	**1**	**0**	**0**
1	**0**	**0**	**0**	**0**	**0**	**0**
1	**0**	**1**	**0**	**0**	**1**	**0**
1	**1**	**0**	**0**	**0**	**0**	**0**
1	**1**	**1**	**0**	**0**	**0**	**1**

PIN DIAGRAM FOR IC 74150:



PIN DIAGRAM FOR IC 74154:



PROCEDURE:

(i) Connections are given as per circuit diagram.
(ii) Logical inputs are given as per circuit diagram.
(iii) Observe the output and verify the truth table.

RESULT:

Hence designed and implemented multiplexer and demultiplexer using logic gates and study of IC 74150 and IC 74154

DESIGN AND IMPLEMENTATION OF ENCODER AND DECODER

EXPERIMENT:14 **DATE:**

AIM:

To design and implement encoder and decoder using logic gates and study of IC 7445 and IC 74147.

COMPONENTS AND EQUIPMENTS REQUIRED:

S.No.	COMPONENT	SPECIFICATION	QTY
1.	3 I/P NAND GATE	IC 7410	2
2.	OR GATE	IC 7432	3
3.	NOT GATE	IC 7404	1
2.	IC TRAINER KIT	-	1
3.	PATCH CORDS	-	27

THEORY:

ENCODER:

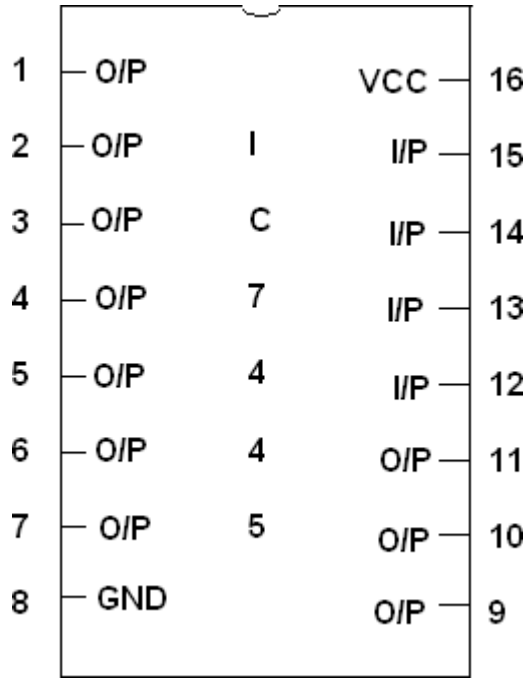
An encoder is a digital circuit that perform inverse operation of a decoder. An encoder has 2^n input lines and n output lines. In encoder the output lines generates the binary code corresponding to the input value. In octal to binary encoder it has eight inputs, one for each octal digit and three output that generate the corresponding binary code. In encoder it is assumed that only one input has a value of one at any given time otherwise the circuit is meaningless. It has an ambiguila that when all inputs are zero the outputs are zero. The zero outputs can also be generated when D0 = 1.

DECODER:

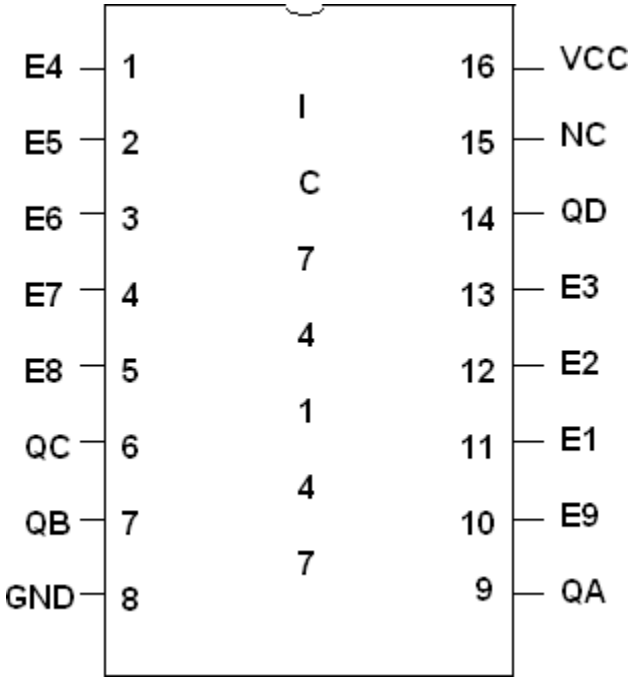
A decoder is a multiple input multiple output logic circuit which converts coded input into coded output where input and output codes are different. The input code generally has fewer bits than the output code. Each input code word produces a different output code word i.e there is one to one mapping can be expressed in truth table. In the block diagram of decoder circuit the encoded information is present as n input producing 2^n possible outputs. 2^n output values are from 0 through out $2^n - 1$.

PIN DIAGRAM FOR IC 7445:

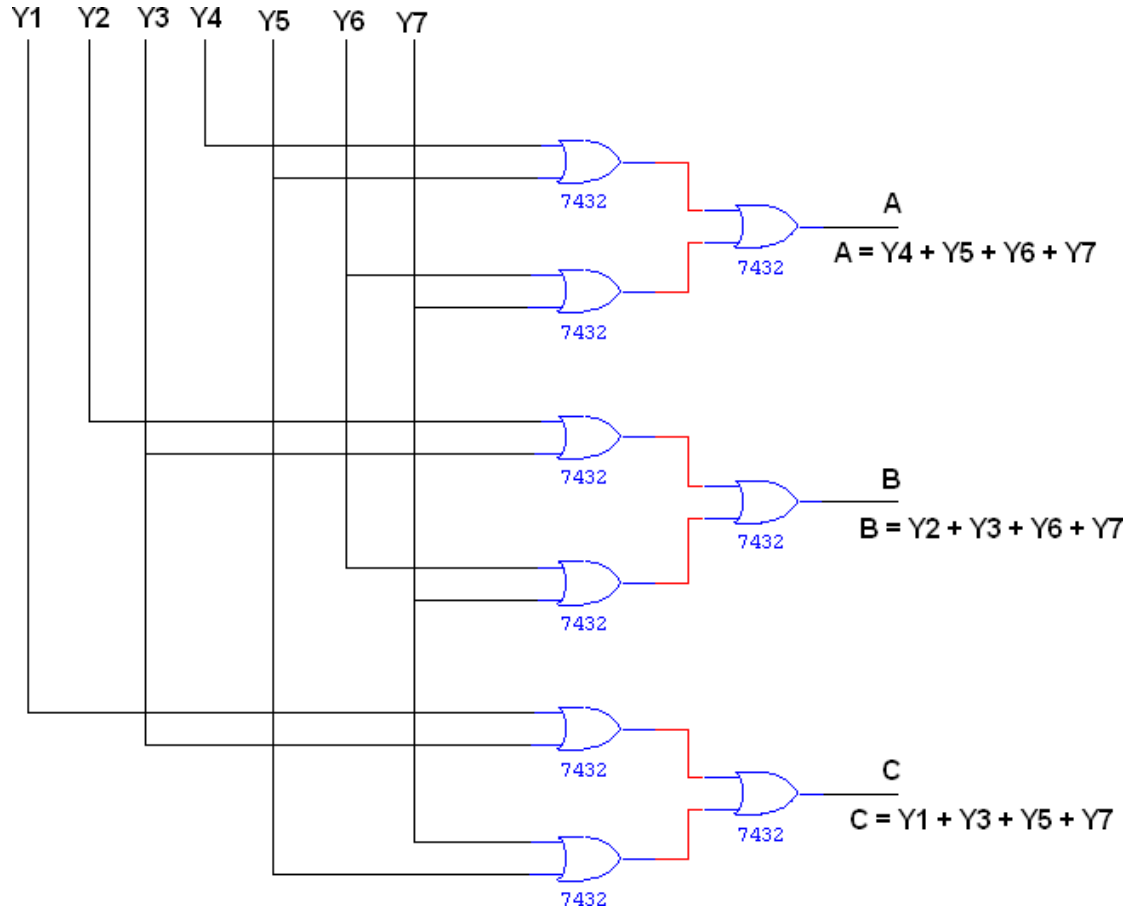
BCD TO DECIMAL DECODER:



PIN DIAGRAM FOR IC 74147:



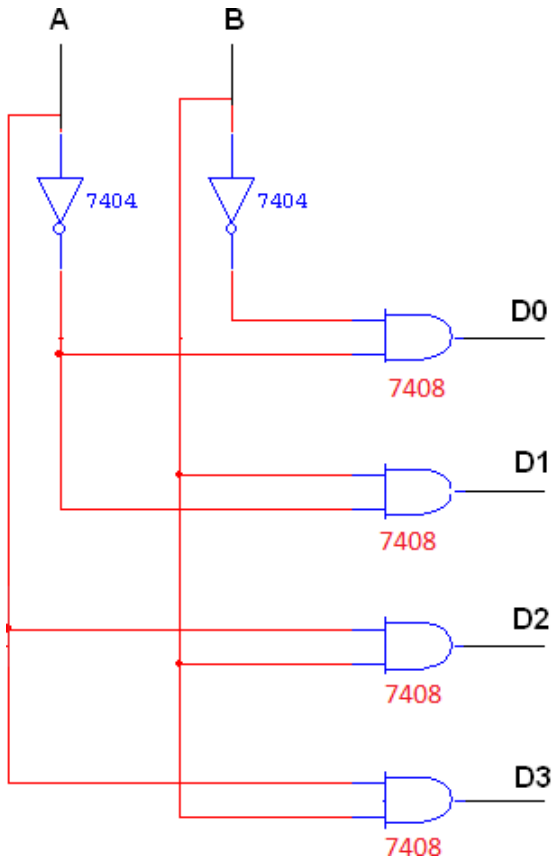
LOGIC DIAGRAM FOR ENCODER:



TRUTH TABLE:

INPUT							OUTPUT		
Y1	**Y2**	**Y3**	**Y4**	**Y5**	**Y6**	**Y7**	**A**	**B**	**C**
1	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
0	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**1**	**1**
0	**0**	**0**	**1**	**0**	**0**	**0**	**1**	**0**	**0**
0	**0**	**0**	**0**	**1**	**0**	**0**	**1**	**0**	**1**
0	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**1**	**0**
0	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**

LOGIC DIAGRAM FOR DECODER:



TRUTH TABLE:

INPUT		OUTPUT			
A	**B**	**D0**	**D1**	**D2**	**D3**
0	**0**	**1**	**0**	**0**	**0**
0	**1**	**0**	**1**	**0**	**0**
1	**0**	**0**	**0**	**1**	**0**
1	**1**	**0**	**0**	**0**	**1**

PROCEDURE:

(i) Connections are given as per circuit diagram.
(ii) Logical inputs are given as per circuit diagram.
(iii) Observe the output and verify the truth table

RESULT:

Hence designed and implemented encoder and decoder using logic gates and study of IC 7445 and IC 74147.

CONSTRUCTION AND VERIFICATION OF 4 BIT RIPPLE COUNTER AND MOD 10/MOD 12 RIPPLE COUNTER

EXPERIMENT:15 **DATE:**

AIM:

To design and verify 4 bit ripple counter mod 10/ mod 12 ripple counter.

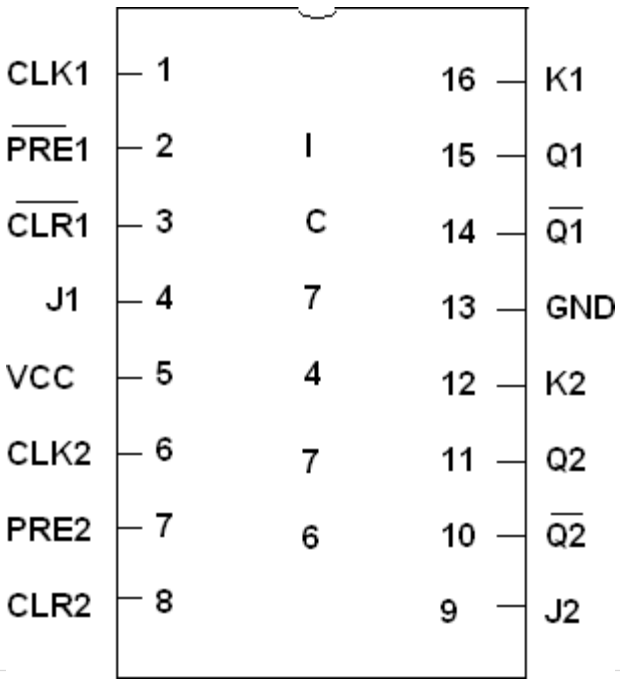
COMPONENTS AND EQUIPMENTS REQUIRED:

S.No.	COMPONENT	SPECIFICATION	QTY
1.	JK FLIP FLOP	IC 7476	2
2.	NAND GATE	IC 7400	1
3.	IC TRAINER KIT	-	1
4.	PATCH CORDS	-	30

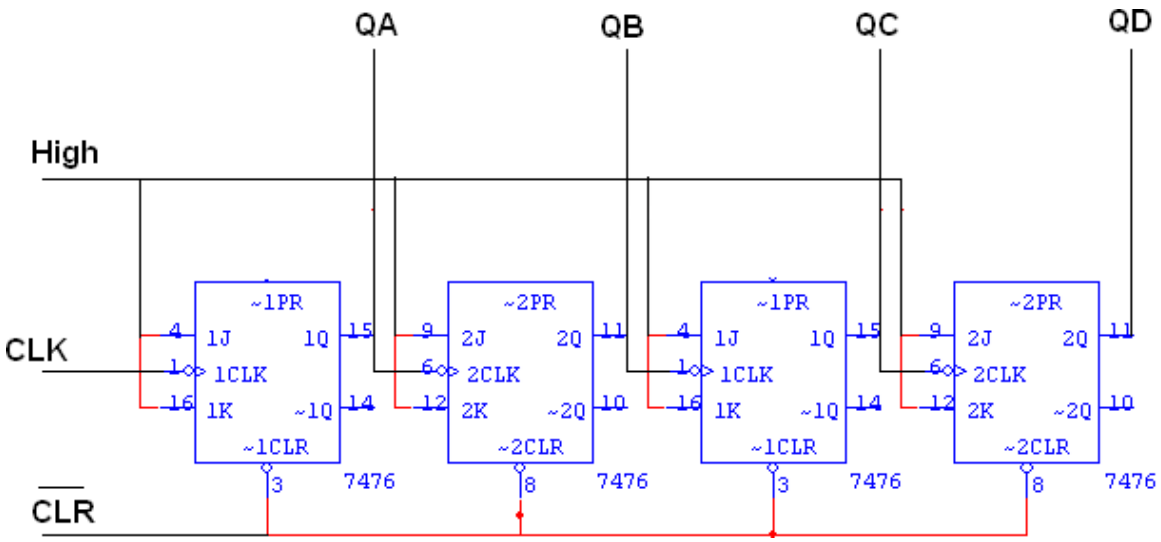
THEORY:

A counter is a register capable of counting number of clock pulse arriving at its clock input. Counter represents the number of clock pulses arrived. A specified sequence of states appears as counter output. This is the main difference between a register and a counter. There are two types of counter, synchronous and asynchronous. In synchronous common clock is given to all flip flop and in asynchronous first flip flop is clocked by external pulse and then each successive flip flop is clocked by Q or Q output of previous stage. A soon the clock of second stage is triggered by output of first stage. Because of inherent propagation delay time all flip flops are not activated at same time which results in asynchronous operation.

PIN DIAGRAM FOR IC 7476:



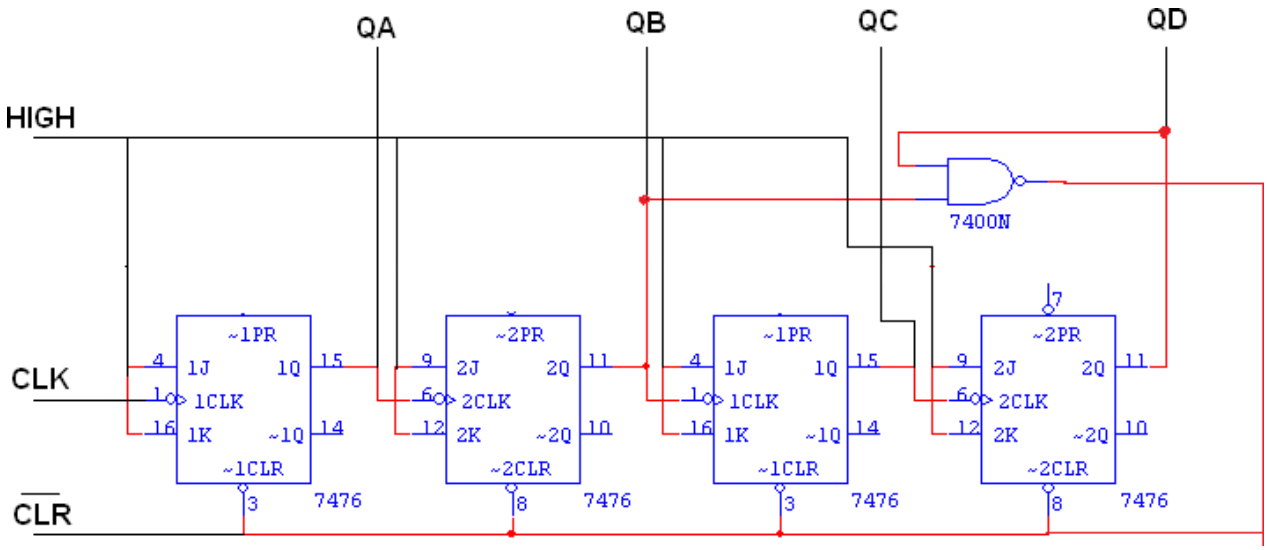
LOGIC DIAGRAM FOR 4 BIT RIPPLE COUNTER:



TRUTH TABLE:

CLK	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1

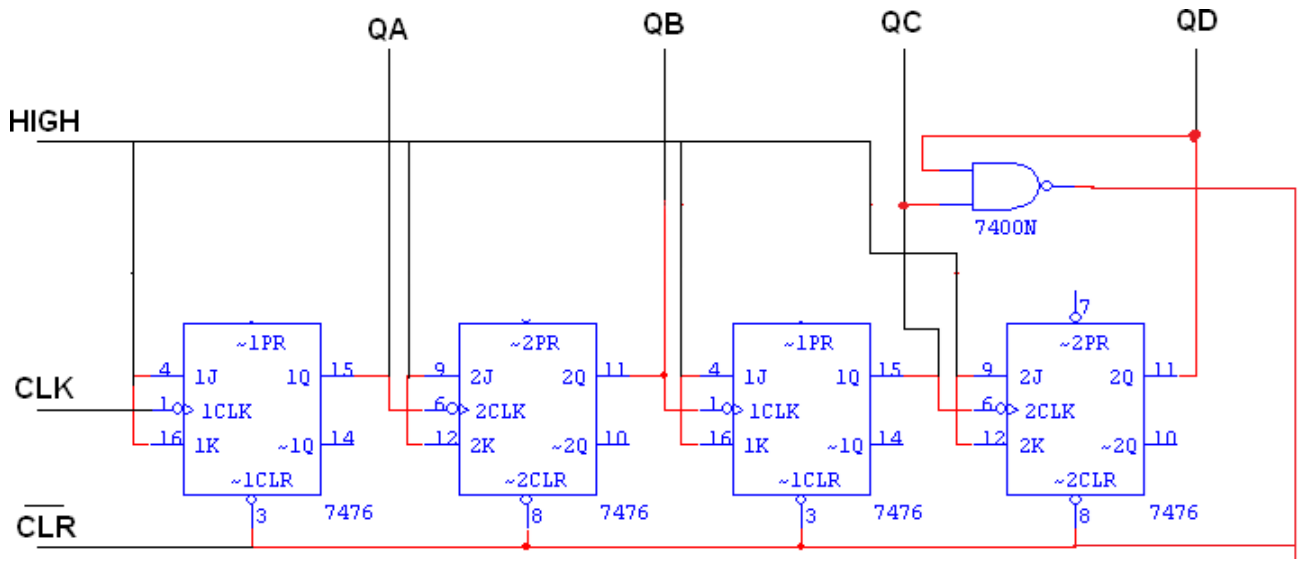
LOGIC DIAGRAM FOR MOD - 10 RIPPLE COUNTER:



TRUTH TABLE:

CLK	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	0	0	0

LOGIC DIAGRAM FOR MOD - 12 RIPPLE COUNTER:



TRUTH TABLE:

CLK	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	0	0

PROCEDURE:

(i) Connections are given as per circuit diagram.
(ii) Logical inputs are given as per circuit diagram.
(iii) Observe the output and verify the truth table.

RESULT:

Hence designed and verified 4 bit ripple counter mod 10/ mod 12 ripple counter.

DESIGN AND IMPLEMENTATION OF 3 BIT SYNCHRONOUS UP/DOWN COUNTER

EXPERIMENT:16 **DATE:**

AIM:

To design and implement 3 bit synchronous up/down counter.

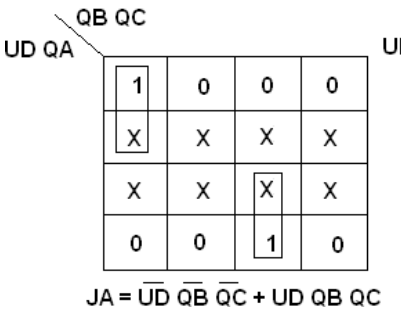
COMPONENTS AND EQUIPMENTS REQUIRED:

S.No.	COMPONENT	SPECIFICATION	QTY.
1.	JK FLIP FLOP	IC 7476	2
2.	3 I/P AND GATE	IC 7411	1
3.	OR GATE	IC 7432	1
4.	XOR GATE	IC 7486	1
5.	NOT GATE	IC 7404	1
6.	IC TRAINER KIT	-	1
7.	PATCH CORDS	-	35

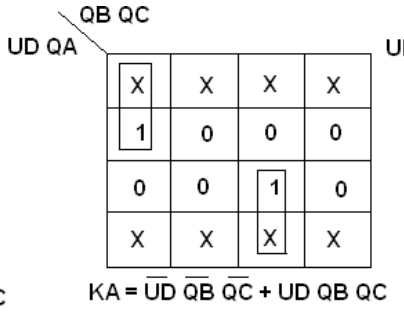
THEORY:

A counter is a register capable of counting number of clock pulse arriving at its clock input. Counter represents the number of clock pulses arrived. An up/down counter is one that is capable of progressing in increasing order or decreasing order through a certain sequence. An up/down counter is also called bidirectional counter. Usually up/down operation of the counter is controlled by up/down signal. When this signal is high counter goes through up sequence and when up/down signal is low counter follows reverse sequence.

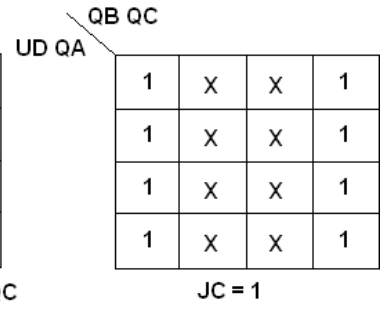
K MAP



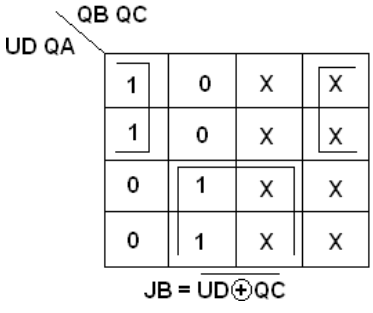
JA = $\overline{UD}\ \overline{QB}\ \overline{QC}$ + UD QB QC



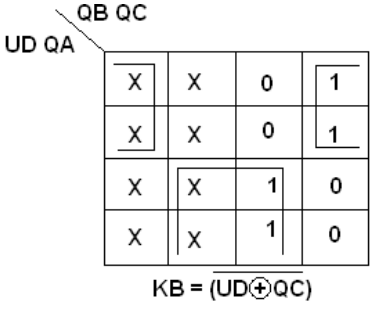
KA = $\overline{UD}\ \overline{QB}\ \overline{QC}$ + UD QB QC



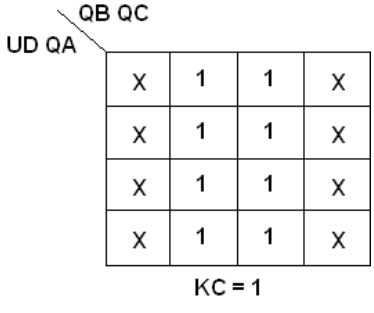
JC = 1



JB = $\overline{UD \oplus QC}$

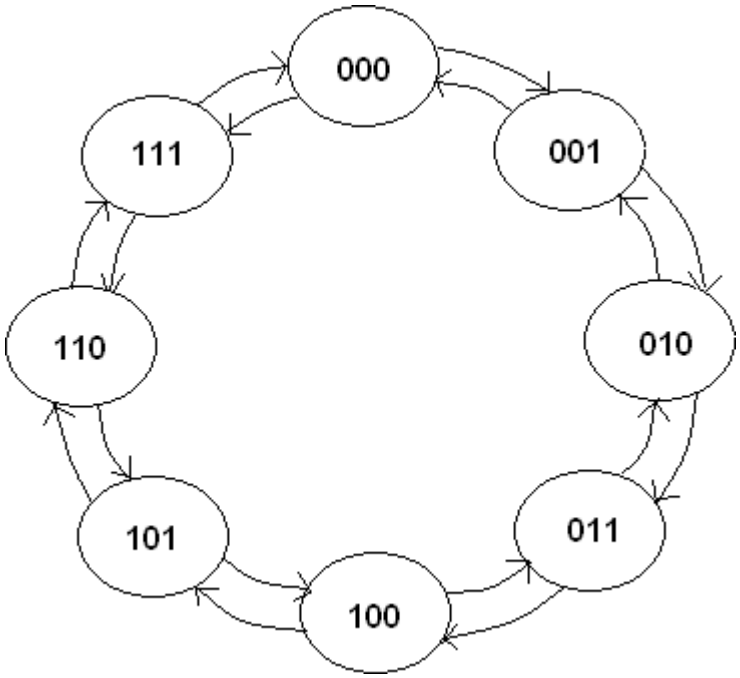


KB = $\overline{(UD \oplus QC)}$



KC = 1

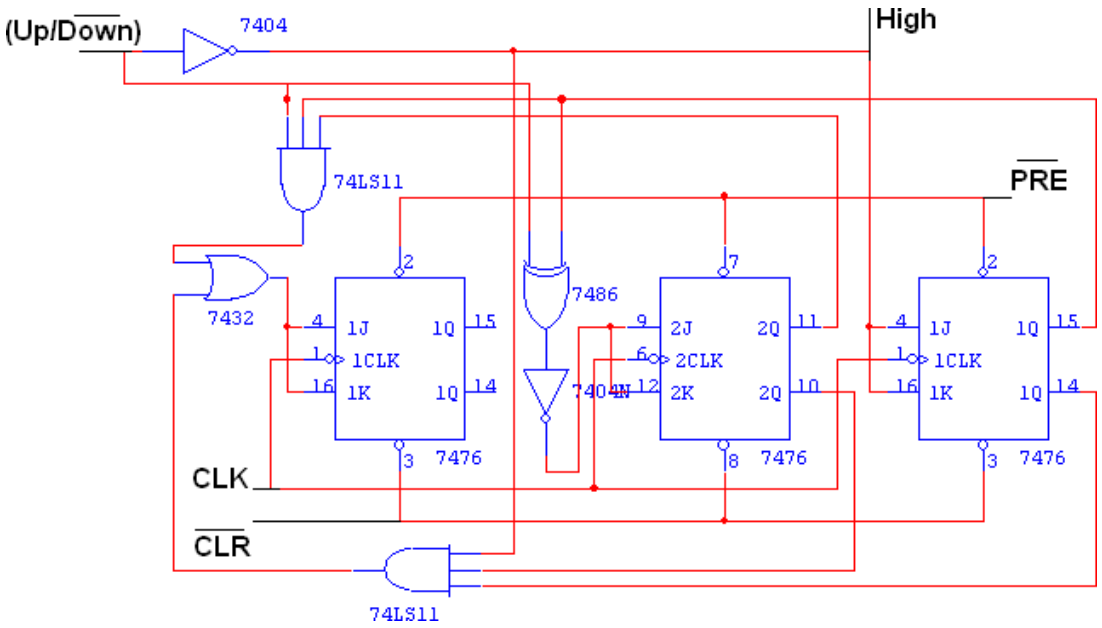
STATE DIAGRAM:



CHARACTERISTICS TABLE:

Q	Q_{t+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

LOGIC DIAGRAM:



TRUTH TABLE:

Input Up/Down	Present State Q_A Q_B Q_C			Next State Q_{A+1} Q_{B+1} Q_{C+1}			A J_A	A K_A	B J_B	B K_B	C J_C	C K_C
0	0	0	0	1	1	1	1	X	1	X	1	X
0	1	1	1	1	1	0	X	0	X	0	X	1
0	1	1	0	1	0	1	X	0	X	1	1	X
0	1	0	1	1	0	0	X	0	0	X	X	1
0	1	0	0	0	1	1	X	1	1	X	1	X
0	0	1	1	0	1	0	0	X	X	0	X	1
0	0	1	0	0	0	1	0	X	X	1	1	X
0	0	0	1	0	0	0	0	X	0	X	X	1
1	0	0	0	0	0	1	0	X	0	X	1	X
1	0	0	1	0	1	0	0	X	1	X	X	1
1	0	1	0	0	1	1	0	X	X	0	1	X
1	0	1	1	1	0	0	1	X	X	1	X	1
1	1	0	0	1	0	1	X	0	0	X	1	X
1	1	0	1	1	1	0	X	0	1	X	X	1
1	1	1	0	1	1	1	X	0	X	0	1	X
1	1	1	1	0	0	0	X	1	X	1	X	1

PROCEDURE:

(i) Connections are given as per circuit diagram.
(ii) Logical inputs are given as per circuit diagram.
(iii) Observe the output and verify the truth table.

RESULT:

Hence designed and implemented 3 bit synchronous up/down counter